DESIGN AND MODELING OF RADIATION HARDENED LDMOSFET FOR SPACE CRAFT POWER SYSTEMS

by

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ABSTRACT

NASA missions require innovative power electronics system and component solutions with long life capability, high radiation tolerance, low mass and volume, and high reliability in space environments. Presently vertical double-diffused MOSFETs (VDMOS) are the most widely used power switching device for space power systems. It is proposed that a new lateral double-diffused MOSFET (LDMOS) designed at UCF can offer improvements in total dose and single event radiation hardness, switching performance, development and manufacturing costs, and total mass of power electronics systems. Availability of a hardened fast-switching power MOSFET will allow space-borne power electronics to approach the current level of terrestrial technology, thereby facilitating the use of more modern digital electronic systems in space.

It is believed that the use of a p+/p-epi starting material for the LDMOS will offer better hardness against single-event burnout (SEB) and single-event gate rupture (SEGR) when compared to vertical devices fabricated on an n+/n-epi material. By placing a source contact on the bottom-side of the p+ substrate, much of the hole current generated by a heavy ion strike will flow away from the dielectric gate, thereby reducing electrical stress on the gate and decreasing the likelihood of SEGR. Similarly, the device is hardened against SEB by the redirection of hole current away from the base of the device’s parasitic bipolar transistor. Total dose hardness is achieved by the use of a standard complementary metal-oxide semiconductor (CMOS) process that has shown proven hardness against total dose radiation effects.
Dedicated to my wife Carrie and my sons Michael and Brendan.
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# TABLE OF CONTENTS

LIST OF FIGURES .......................................................................................................... vii
LIST OF TABLES ............................................................................................................. viii
LIST OF ACRONYMS AND ABBREVIATIONS .......................................................... ix

1  CHAPTER ONE: INTRODUCTION ......................................................................1
   1.1  Motivation ....................................................................................................2
   1.2  Discussion of Harmful Radiation Effects ....................................................3
       1.2.1 Carrier Generation and Collection ...................................................4
       1.2.2 Dose Rate Events .............................................................................6
       1.2.3 Single Event Effects .........................................................................8
           1.2.3.1 Single Event Burnout ........................................................9
           1.2.3.2 Single Event Gate Rupture ..............................................10
       1.2.4 Total Dose Effects ..........................................................................11
   1.3  Radiation Hardening ..................................................................................12

2  CHAPTER TWO: DEVICE CONCEPT ...............................................................14
   2.1  Inherent Vulnerability of the VDMOS ......................................................14
   2.2  The Hardened LDMOS .............................................................................16
   2.3  Device Design Considerations ..................................................................18

3  CHAPTER THREE: MODELING AND DESIGN ...............................................22
   3.1  Fabrication Modeling .................................................................................23
   3.2  Electrical Modeling ....................................................................................29
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>Design Optimization</td>
<td>38</td>
</tr>
<tr>
<td>3.4</td>
<td>Mask Layout</td>
<td>46</td>
</tr>
<tr>
<td>4</td>
<td>CHAPTER FOUR: EXPERIMENTAL RESULTS</td>
<td>47</td>
</tr>
<tr>
<td>5</td>
<td>CHAPTER FIVE: SUMMARY AND FUTURE WORK</td>
<td>52</td>
</tr>
<tr>
<td>5.1</td>
<td>Future Work</td>
<td>52</td>
</tr>
<tr>
<td>5.2</td>
<td>Summary</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td>LIST OF REFERENCES</td>
<td>54</td>
</tr>
</tbody>
</table>
LIST OF FIGURES

Figure 1: VDMOS Current Conduction Paths ................................................................. 11
Figure 2: VDMOS and Equivalent Circuit During Heavy Ion Irradiation ...................... 15
Figure 3: LDMOS and Equivalent Circuit During Heavy Ion Irradiation ...................... 17
Figure 4: UCF LDMOS Dimensional Variables ............................................................. 19
Figure 5: Establishment of Baseline Design .................................................................. 27
Figure 6: FLOOPS-generated LDMOS Structure ......................................................... 28
Figure 7: Circuit Used to Model Breakdown Voltage .................................................. 30
Figure 8: Typical IV Plot for BV Simulation ................................................................. 30
Figure 9: Electric Field at Avalanche Showing RESURF Effect ................................... 31
Figure 10: Electric Field and Potential Distributions at Avalanche Breakdown .............. 32
Figure 11: Circuit Used to Model On-Resistance ......................................................... 33
Figure 12: Typical IV Plot for On-Resistance Simulation ............................................ 34
Figure 13: Electron Current Density Distribution in the On-State ................................. 35
Figure 14: Circuit Used to Model Threshold Voltage .................................................. 36
Figure 15: Typical IV Plot for Threshold Voltage Simulation ...................................... 37
Figure 16: Normalized LDD Dose versus BV and R_{DS-on} ......................................... 39
Figure 17: Normalized LDD Implant Dose versus Threshold Voltage ......................... 40
Figure 18: Normalized P-Body Implant Dose versus V_{th} and R_{DS-on} ...................... 41
Figure 19: Normalized P-Body Implant Dose versus BV ............................................. 42
Figure 20: Normalized P-Body/Gate Overlap versus BV ........................................... 43
Figure 21: Normalized P-Body/Gate Overlap versus $V_{th}$ and $R_{DS-on}$.................................44

Figure 22: Experimentally Obtained IV Plot.................................................................47

Figure 23: Threshold Voltage Measurement ...............................................................48

Figure 24: Breakdown Voltage Measurement ...............................................................49
**LIST OF TABLES**

Table 1: Effects of Key Design Variables on Performance..............................................21

Table 2: Fabrication Process Parameters for FLOOPS Simulator........................................25

Table 3: LDMOS Fabrication Process..............................................................................26

Table 4: Experimental Notes for One Wafer ....................................................................50
# LIST OF ACRONYMS AND ABBREVIATIONS

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV</td>
<td>Breakdown Voltage</td>
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<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
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<tr>
<td>DUT</td>
<td>Device Under Test</td>
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<tr>
<td>LDD</td>
<td>Lightly Doped Drain</td>
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<td>LDMOS</td>
<td>Lateral Double-Diffused MOSFET</td>
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<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field Effect Transistor</td>
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<td>RDS-ON</td>
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<td>SCR</td>
<td>Space Charge Region</td>
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<td>Single Event Burnout</td>
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<td>Single Event Effects</td>
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<td>Single Event Gate Rupture</td>
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<td>Vertical Double-Diffused MOSFET</td>
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<tr>
<td>VTH</td>
<td>Threshold Voltage</td>
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1 

CHAPTER ONE: INTRODUCTION

In an effort to facilitate the modernization of space-borne power systems, the UCF Power Semiconductor Research Laboratory is developing a new class of rad-hard power switch – a Lateral Double-Diffused Metal-Oxide-Semiconductor Field Effect Transistor (LDMOSFET or LDMOS). This switch is intended to provide the radiation hardness and electrical characteristics necessary to implement low-voltage, fast switching power supplies in space, and therefore enable the use of more modern electronics throughout all electrical systems in spacecraft. The use of this type of modern power system will result in an overall increase in power efficiency and enable longer battery life, increased computing performance, reduced mass, and a simplification of electrical system design through greater compatibility with modern electronics. The new LDMOS is also designed to be compatible with the conventional complementary metal-oxide-semiconductor (CMOS) fabrication process used by nearly all semiconductor manufacturers and shown to provide suitable radiation tolerance. Use of this ubiquitous fabrication technology should result in decreased development and manufacturing costs when compared to the specialized processes required to fabricate the current class of commercial devices.
1.1 Motivation

Digital circuits have largely driven the advancement of all types of technology that find use in spacecraft. A space satellite’s computers, sensors, communications and control systems all rely on the same basic digital components. Across the history of their development, digital components have become smaller and faster, with ever increasing density and complexity, however these improvements have not been fully realized in space-borne applications due in large part to the lack of suitable power systems. Today’s microprocessors operate at ever decreasing voltages and increasing currents, and as the requirements of these systems have changed, the technology of power electronics must become more advanced in order to keep pace.

There is a long-standing disparity between terrestrial electronics and radiation hardened (rad-hard) electronics in terms of performance and cost. This results in space craft being equipped with slower computers, less efficient power systems, and electronics of higher mass and volume than would be found on Earth in similar applications. Additionally, the cost of commercial radiation-hardened electronics remains very high due to low sales volume, a long development cycle, and special design considerations required to reliably harden semiconductor devices against the harmful ionizing radiation present in space. The cost of developing specially hardened components, coupled with the risk inherent in a niche market, has resulted in an overall lack of competition among manufacturers of this specialized technology. This lack of driving market forces has
resulted in an overall lack of development of new technologies specifically in the arena of power devices.

The heart of these power systems is the metal-oxide-semiconductor field effect transistor (MOSFET). The performance of modern low-voltage power supplies is most affected by the technology of these transistors. When compared with older systems, the power MOSFETs required for use in modern digital systems must switch at higher frequencies and exhibit lower conduction losses and internal capacitance. There is presently lack of rad-hard power transistors with these characteristics. Although modern sub-micron CMOS technology shows proven radiation tolerance, radiation-hardened power electronics fail to meet the requirements of state-of-the-art digital circuits and therefore limit their use.

1.2 Discussion of Harmful Radiation Effects

The two major classifications of observable radiation effects are “single-event” phenomena (SEP) and “dose rate” phenomena. SEP by definition are associated with exposure to particle radiation, whereas dose rate phenomena are produced by electromagnetic pulses. Both types of event can produce recoverable “soft errors” or permanently damaging “hard errors”, however the occurrence of permanent damage is more often associated with SEP [1]. The long term effects of both phenomena are
classified separately as “total dose” effects and can lead to problems ranging from diminished performance to complete circuit failure.

### 1.2.1 Carrier Generation and Collection

Both types of radiation events occur due to the generation and subsequent collection of radiation-induced free carriers in the semiconductor. The mechanisms by which carriers are produced are all related to the transfer of energy from radiation to the semiconductor. The energy transfer of an EM radiation dose is measured in units of rads(element) per second. Rad is a material specific unit, corresponding to the amount of ionizing radiation required to transfer 0.1 $\mu$J of energy per gram of material. For silicon, such a dose rate would be expressed as 1 rad(Si)/s. Energy deposited by particle radiation is generally expressed per unit length along its path in terms of linear energy transfer (LET), which is also material specific. LET is measured in units of eVcm$^{-2}$mg$^{-1}$. Heavier ions have higher LET values than lighter ions of the same energy [1].

In the case of high energy photons (X-rays, $\gamma$-rays), the three associated carrier generation mechanisms are direct EHP production, the photoelectric effect, and Compton scattering. In the case of direct EHP production, the entire energy of the photon is absorbed by an electron in the valence band, thereby allowing it to enter the conduction band and leave a hole behind. In the case of Compton scattering, the energy and momentum of the photon is transferred to an electron, but the electron in turn recoils,
giving back some kinetic energy and sending the photon off in a new direction. If enough energy is absorbed by the electron, then both an EHP and a residual photon of decreased frequency are produced [2]. For a wide spectrum of photon energy (<0.1 to >10 MeV), Compton scattering is the dominant carrier generation mechanism in silicon [3]. Generally, exposure to EM radiation occurs over the entire area of the device, and results in excess carriers being generated more or less uniformly throughout.

Carrier generation associated with particle radiation differs in that the incident particle produces a high concentration of free carriers only within a radius of <1 micrometer along its path as it penetrates the semiconductor. Atoms within the crystal lattice may be displaced, leaving open bonds which produce free electrons and possibly forming a permanent lattice defect. Kinetic energy may also be transferred directly to electrons, accelerating them into the conduction band. A third carrier generation mechanism is indirect ionization from nuclear decay caused by collision between the incident particle and an atom within the lattice [1][4][5]. In this case, the decayed particles may transfer more kinetic energy to neighboring atoms than was present in the original collision, generating a high number of free electrons. The decayed atoms may also remain trapped within the lattice, causing a displacement defect and localized ionization.

The most disruptive and destructive events associated with ionizing radiation occur as a result of the high current levels associated with the collection of radiation-induced excess carriers. Depending on the relative number of free carriers produced by the radiation event, different recombination mechanisms with different recombination
rates may dominate. In the case where the number of generated carriers is less than the background doping concentration, the associated region is said to be under low level injection (LLI). The dominant recombination mechanism under LLI is Shockley-Read-Hall (SRH) recombination, with carrier lifetimes on the order of 1-1000 microseconds. However, energy transferred by ionizing radiation can generate mobile carriers at the rate of one electron-hole pair (EHP) per 3.6 eV in silicon. Given that prolonged exposure to radiation with energy on the order of several GeV may be encountered, the radiation-induced free carrier concentration can easily become equal to the background doping concentrations found in silicon devices. In this case, the semiconductor is said to be under high level injection (HLI), and the dominant recombination mechanism becomes Auger recombination, which occurs at a much faster rate than SRH. Modeling of ionizing radiation effects should therefore include models for these physical mechanisms when possible.

1.2.2 Dose Rate Events

Exposure to an EM pulse generates carriers more or less uniformly throughout a large exposed area near the surface of the device. Assuming uniform carrier generation across the affected area, the induced photocurrent density associated with dose rate phenomena can be expressed as,
\[ J(t) = qWG(t) + \int_{0}^{t} G(t - \lambda) \left[ \frac{D_n \exp(-\frac{\lambda}{\tau_n}) + D_p \exp(-\frac{\lambda}{\tau_p})}{\sqrt{\pi \lambda}} \right] d\lambda \]  \hspace{1cm} (1)

where \( W \) = depletion region width (cm), \( G \) = minority carrier generation rate (cm\(^{-3}\)s\(^{-1}\)), \( \lambda \) = photon wavelength, and \( D_n, D_p \) and \( \tau_n, \tau_p \) are the minority diffusion coefficients and carrier lifetimes for electrons and holes respectively [1]. Since both the generation rate and photon wavelength are dependent on the radiation type and dose, which are assumed to be uncontrollable, and the depletion region width is assumed fixed for a given blocking voltage, the only option toward reducing current levels is to reduce the minority carrier lifetime. Carrier lifetime decreases in highly doped silicon, and therefore the use of high doping concentration in sensitive device regions is one method of hardening against EM radiation exposure [1].

The effects of most dose rate events are also minimized by the fact that the exposure duration is usually short compared to the amount of time required for drift mechanisms to transport the generated charge out of the device. For this reason, the current levels commonly associated with dose rate events remain low enough to cause no permanent damage, and the device may resume normal operation after the event. However, dose rate hard errors can occur, wherein the device becomes permanently damaged. In cases where the induced photocurrent density is very high, the resulting generation of heat can melt metal interconnects or break wirebonds away from bondpad interfaces. These effects may become self-compounding. As current carrying wirebonds are broken, the remaining wires are forced to carry additional current and therefore
undergo more thermal stress. This presents a long term reliability concern as hotspots form in the device and eventually lead to thermal runaway and second breakdown, resulting in permanent destruction [1].

1.2.3 Single Event Effects

In contrast to the more or less uniform current generated by dose rate events, SEP introduce a high concentration of free carriers along a narrow path that can traverse deep into silicon. This path becomes a highly conductive region that can penetrate p-n junctions, and is sometimes referred to as an “ion shunt”. The difference between effects associated with single event phenomena and dose rate phenomena are due to this difference in the spatial distribution of injected carriers. Depending on the type of device and the biasing conditions at the time of radiation exposure, the resulting currents can trigger destructive effects such as single-event burnout (SEB) and single-event gate rupture (SEGR).

When an energetic particle traverses a p-n junction in the blocking state, the depletion region along the ion shunt is temporarily removed. However, depletion regions across p-n junctions a short distance away from the shunt are still able to be maintained. This results in a localized area of high drift current density, which in turn can produce further carrier generation through avalanche multiplication and carrier-induced scattering. The amount of collected charge may be significantly greater than the charge introduced
along the ion path if high level injection occurs, as is commonly the case during destructive events. Whether or not the device is destroyed depends on a combination of factors including the energy of the incident ion, the biasing conditions at the time of the event, and also the location of the event with respect to the device’s doping profile.

1.2.3.1 Single Event Burnout

Single-event burnout (SEB) occurs primarily in power transistors used in space environments. This effect occurs when high current levels caused by an incident heavy ion force the device into thermal runaway. The mechanism is activation of the parasitic bipolar transistor present in conventional vertical power MOSFET designs, an example of which is shown in Figure 1.

Vertical power MOSFETs are created on a lightly-doped n- epitaxial later which resides on an n+ substrate. The epi layer must be lightly doped in order to support the required breakdown voltage across the p-plug/epi junction. The lightly doped epi, together with a thin and relatively heavily doped p-plug, form a bipolar transistor with potentially high current gain. When a heavy ion shunts the p-n junctions through the device, the blocking voltage is no longer maintained and current flows freely between the drain and source regardless of gate voltage. Electron current is collected at the positively biased substrate contact, and hole current flows through the p-plug and is then collected at the body contact which is shorted to the source. As current levels increase, the
resistance in the p-body causes a voltage drop across the source/p-body junction. When this potential reaches ~0.7 V the junction becomes forward biased, placing the parasitic bipolar transistor in the forward-active operating area. As the base current is amplified, a base pushout effect occurs as the device enters HLI, and the peak electric field shifts away from the base-collector junction toward the n+/n-epi junction. The resulting strong electric field then generates additional free carriers via avalanche multiplication, which in turn generates more supply current. This positive feedback mechanism continues until the device enters second breakdown and is destroyed. Whether or not the device enters this destructive state is based on the source-drain (collector-base) bias for a given ion strike, and also the doping profile of the device [6][7][8].

1.2.3.2 Single Event Gate Rupture

Single event gate rupture (SEGR) is a condition in which the gate dielectric fails under extreme electrical stress. As excess carriers are collected in a VDMOS following an ionized particle strike, electrons are drawn to the bottom-side n+ drain while holes are drawn to the p-type channel region underneath the gate oxide. As positive charge accumulates at the Si/SiO2 interface, an electric field forms between that interface and the gate metal. The strength of this electric field is dependent on the hole current density under the gate and the bias on the gate terminal. If the strength of the electric field reaches the critical breakdown field of the thin oxide layer, the gate dielectric will lose its
insulating properties and begin conducting current. Once this occurs, a permanent leakage path forms across the gate oxide and the device will no longer function [6].

Cross-sectional view of a vertical power MOSFET and the current conduction paths associated with a heavy ion strike. The parasitic bipolar transistor between the source and drain can produce destructive current when activated by ionizing radiation. The strong electric field associated with accumulated charge under the gate can lead to SEGR [6].

Figure 1: VDMOS Current Conduction Paths

1.2.4 Total Dose Effects

Total dose effects are the result of repeated exposure to ionizing radiation. The most common such effects are the creation of hotspots due to local interconnect failure, mentioned previously, and threshold voltage shifts and increased leakage current in MOS devices. Threshold voltage shifts are attributed to the collection of radiation-induced charge within the gate oxide and along the Si/SiO2 interface. At the interface, dangling
bonds are present between the amorphous oxide and the silicon crystal lattice. These interface states act as charge trapping centers by allowing carriers to exist at energy levels that fall within the normally forbidden energy bandgap. Oxygen deficiency centers within the dielectric also serve as charge trapping sites.

Trapped charges can be either positive or negative, depending on their energy state. Positive trapped charge lowers the threshold voltage of NMOS devices, while negative trapped charge has the same effect for PMOS devices. Threshold voltage shifts over time can become so dramatic that transistors enter an on-state when zero external gate voltage is applied. In this case, control over the device is lost and the associated circuit no longer maintains proper operation. In addition to altering threshold voltage, another adverse effect of trapped charge is the formation of conductive layers underneath or through the gate oxide, resulting in a direct leakage current path between the source, gate and drain. In many cases, the high temperatures involved with radiation induced current can have a reparative annealing effect, driving trapped charges out of the oxide. In other cases, the positive and negative trapped charges balance each other in such a way as to produce a negligible net effect.

1.3 Radiation Hardening

Catastrophic dose rate events can be effectively prevented through the use of shielding in both the device package and the surrounding larger system. This is because
EM radiation can be severely attenuated with relatively thin layers of metal. The use of gold doping has also been found to increase EM radiation hardness by speeding up the associated recombination mechanisms. Oxidation methods have been developed to reduce the number of interface charge trapping sites, assisting in hardening against total dose effects, as does the minimization of gate dielectric thickness and area. Techniques for hardening against heavy ions are limited to the constraints of device structures and fabrication technology.

In general, devices are designed to prevent the activation of parasitic bipolar elements. To prevent SEB, designers have relied mainly on a brute force method of using MOSFETs with much higher breakdown voltages than are required by the system [9][10][11]. For instance, a system operating at 40 V may be fitted with a switch rated at 150 V. This has the adverse effect of introducing a switch with higher on-resistance and capacitance, thereby increasing conduction and switching losses and limiting system performance. Designers also attempted to counteract SEB by using large current-limiting resistors in series with the switch, however the internal capacitance of the VDMOS can be charged with enough energy to induce SEB regardless of the external circuit, limiting the effectiveness of this method. To date, there is no published technique to effectively harden against single event gate rupture.
2 CHAPTER TWO: DEVICE CONCEPT

2.1 Inherent Vulnerability of the VDMOS

Conventional rad-hard power MOSFETs use a vertical double-diffused structure (VDMOSFET or VDMOS) in which current is conducted through the wafer from top to bottom. These devices are fabricated on an n+ silicon substrate with an n-type epitaxial layer. During operation, a positive voltage is applied to the bottom-side drain, which creates a voltage-sustaining space charge region (SCR) across both the n-drift and p-body regions. When a positive bias is applied to the dielectric gate, an inversion layer forms in the p-body at the semiconductor-dielectric interface, the SCR collapses, and current is allowed to flow freely from drain to source.

The p-body forms the base of the device’s parasitic bipolar transistor and also serves as the sole collection path for hole current in the device, as illustrated in Figure 2. This is why the VDMOS structure is inherently prone to SEB. In the absence of an alternate path, the entire hole current generated by a heavy ion strike must pass through this narrow, highly doped base, resulting in a localized region of dangerously high hole current density. During such an event, the voltage drop across the p-body may be sufficiently high to forward bias the base-emitter junction of the parasitic BJT, thereby causing the device to enter latch-up and be destroyed.
VDMOS structure and equivalent circuit under the condition of heavy ion irradiation. The radiation-induced current is forced to flow through the base of the parasitic n-p-n transistor, as represented by the pulsed current source in the equivalent circuit.

Figure 2: VDMOS and Equivalent Circuit During Heavy Ion Irradiation

The VDMOS structure is also inherently prone to SEGR. This is because of the gate’s proximity to the high hole current densities just mentioned and the fact that the electric field is always pointed toward the gate. It would be better to create a structure in which hole current could be collected across a wider region at lower densities, thereby reducing the forward voltage drop across the base-emitter junction and making the device less susceptible to SEB. To harden against SEGR, it would be better to point the electric field away from the gate and also provide holes with a current path that is far from the gate. These methods could prevent the strong accumulation of holes under the gate dielectric that results in rupture. These are the techniques employed in the LDMOS currently being developed at UCF.
2.2 The Hardened LDMOS

An approximation of the UCF LDMOS and its equivalent circuit is shown in Figure 3. In contrast to the VDMOS, this lateral switch conducts current along the top surface of the silicon wafer and is fabricated on a p+ silicon substrate with a p- epitaxial layer. The top-side source contact is surrounded by a heavily doped p-body. The p+ substrate is tied externally to the top-side source via a bondwire, forming a common ground for the switch. The result is an electric field that points down toward the substrate instead of up toward the gate, and a very large area for the collection of hole current away from the gate. As illustrated in Figure 3, the hole current generated by a heavy ion event will flow to the bottom-side source contact instead of being forced through the base of the parasitic n-p-n transistor. There should be a significant reduction in the maximum hole current density both through the p-body and under the gate, reducing the likelihood of both SEB and SEGR.

The LDMOS offers additional hardness, performance, and market benefits. The LDMOS has a poly gate area roughly half that of a VDMOS in similar application. This results in very low gate charge and capacitance, enabling the LDMOS to be used in low mass, high frequency power converters. The ability to reduce the mass of any space system is highly desirable in terms of cost, and the use of faster switching power supplies might enable the modernization of space-borne digital electronics. Lower gate area also reduces the number of charge trapping sites associated with total dose effects, as does the LDMOS’s compatibility with standard CMOS fabrication processes. Digital electronics
manufactured on a CMOS platform have already shown proven hardness against total
dose radiation. CMOS also offers benefits in terms of reduced design, testing and
manufacturing costs and opens the door for much needed competition in the field of
hardened power electronic devices.

Proposed UCF LDMOS and the equivalent circuit under the condition of heavy ion radiation. The
radiation-induced current is collected at the bottom-side source contact, away from the base of
the parasitic n-p-n transistor, as represented by the equivalent circuit.

Figure 3: LDMOS and Equivalent Circuit During Heavy Ion Irradiation
2.3 Device Design Considerations

An idealized drawing which labels the key design dimensions of the LDMOS structure is shown below in Figure 4. This figure shows one half unit cell of the device. In the actual device, this cell is mirrored and repeated many times, effectively creating hundreds or possibly thousands of discrete devices connected in parallel. This is a standard design technique used to allow power devices to sustain high current levels with minimal resistance and also helps to ensure near-homogeneous conduction across the device. The length of each cell is called the “cell pitch”. This dimension is used in the calculation of specific drain-source on-resistance ($R_{DS-on}$), an important characteristic of power devices which is calculated as electrical resistance per unit area as the device is in the on-state. Area specific resistance at a given gate voltage offers a fair comparison of devices with different current ratings that contain different numbers of parallel unit cells. $R_{DS-on}$ primarily serves as a benchmark to describe efficiency of silicon area utilization – a major cost factor. A key figure of merit (FOM) for power devices is $BV \times R_{DS-on}$. This FOM takes into account the inherent tradeoff between the two characteristics.
The blocking capability of the device is maintained by an n-type lightly-doped drain (LDD) region formed between the gate and the drain contact. The LDD is designed to take advantage of the reduced surface field effect (RESURF) – a common method used in power devices to improve the trade-off between specific on-resistance and breakdown voltage [12]. RESURF is a two-dimensional effect which allows the voltage-sustaining SCR to spread widely across both sides of a p-n junction. The design goal is for the LDD to become fully depleted as the device reaches its breakdown voltage, thereby spreading the electric field across its entire area and reducing the peak electric field at both the junction and the gate. Reducing electrical stress on the gate is an important consideration both in terms of long-term reliability and also total-dose radiation hardness.

Each dimension labeled in Figure 4 has its own effect on key device performance parameters such as breakdown voltage (BV), threshold voltage (V_{th}), and R_{DS-on}. These are the three performance characteristics around which the structure was designed.
During the initial design process it was decided to maintain a constant cell pitch throughout all the designs. This was done in order to simplify mask layout for the first run of devices. In order to maintain a constant cell pitch, the drain and source implant dimensions were varied to accommodate different lengths of the gate and LDD regions. This technique is valid in terms of designing for BV, $V_{th}$, and $R_{DS-on}$, since the contact implants do not noticeably affect these parameters, and the variations in contact region length did not appreciably affect $R_{DS-on}$ calculations. Considering this, Table 1 shows how each of the important design variables is expected to affect device performance.
### Table 1

**Effects of Key Design Variables on Performance**

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<tr>
<th>Design Variable</th>
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<td></td>
<td></td>
<td>$\uparrow$</td>
</tr>
<tr>
<td>$L_p - L_g$</td>
<td>p-body/gate overlap</td>
<td>$\uparrow$ $\ast$</td>
</tr>
<tr>
<td></td>
<td>prevents</td>
<td>$\uparrow$</td>
</tr>
<tr>
<td>$L_{LDD}$</td>
<td>drift region length</td>
<td>$\uparrow$ $\uparrow$</td>
</tr>
<tr>
<td>$N_p$</td>
<td>p-body doping concentration</td>
<td>$\uparrow$</td>
</tr>
<tr>
<td></td>
<td>prevents</td>
<td>$\uparrow$</td>
</tr>
<tr>
<td>$N_{epi}$</td>
<td>epitaxial layer doping</td>
<td>$\downarrow$ $\uparrow$ $\uparrow$</td>
</tr>
<tr>
<td>$N_{LDD}$</td>
<td>drift region doping</td>
<td>$\downarrow$ $\downarrow$</td>
</tr>
</tbody>
</table>

**Key:**
- $\uparrow$ directly related
- $\downarrow$ inversely related
- -- zero or negligible effect
- $\ast$ $V_{th}$ eventually plateaus as determined by $N_p$
3 CHAPTER THREE: MODELING AND DESIGN

The goal of this work is to design a 25 V LDMOS with a threshold voltage of 2.5 volts with minimal gate charge and on-resistance. The design is accomplished using the ISE TCAD v.10 family of software. TCAD is an advanced suite of drafting and simulation tools developed specifically for the design and modeling of semiconductor devices. The TCAD components used during the design process are MDRAW, FLOOPS, and DESSIS. MDRAW is a graphical user interface drafting tool that allows for the rapid creation of multiple design iterations for rough prototyping. FLOOPS is an advanced fabrication process simulator that allows for the fine-tuning of design considerations and process conditions. DESSIS is a numerical simulator used to observe the electrical performance of each design by solving Poisson’s equation and the electron and hole current continuity equations at densely located mesh points throughout the simulated device structure.

The first phase of the design process was to determine a baseline doping profile for a functioning device. This was accomplished by drafting multiple design iterations using MDRAW and then testing their performance using the DESSIS simulator. MDRAW allows for the creation of graded impurity distributions that mimic ion implantation and diffusion, but does not create the detailed non-idealities generated by the fabrication simulator (FLOOPS). The benefit of MDRAW is the speed at which structures may be generated. Several design iterations can be tested using MDRAW and DESSIS in the time required to generate a single structure using FLOOPS. Using this
method, non-functioning designs were tested and discarded using minimal time and resources.

Simulation convergence and solving time was optimized by careful design of the structure’s mesh. The mesh is a network of discrete spatial points at which solutions are generated by the simulator. Fewer mesh points reduce the number of calculations for each solving iteration, but a coarse mesh can lead to convergence problems and also compromise the accuracy of modeling results. A very dense mesh will generally yield accurate solutions, however the solving time may be increased to a point where productivity greatly suffers. In order to balance accuracy and solving time, the mesh was made selectively dense or coarse in different regions of the device. The general technique was to set mesh density in direct proportion to the doping concentration gradient and anticipated electric field across each region. This allows large relatively equipotential regions to be solved quickly, while smaller regions with high electric field are solved with high resolution. In the case of the LDMOS, the highest mesh densities occur at each p-n junction, under the gate oxide, and throughout the LDD region.

3.1 Fabrication Modeling

Once an acceptable baseline doping profile was established using MDRAW, the FLOOPS simulator was used to determine the fabrication process conditions necessary to realize the design. Table 2 details all of the required variables for various steps in the
fabrication process. These variables include mask layer coordinates, species, dose and energy for ion implantations, and time, temperature and ambient conditions for thermal oxidation, implant drives, and anneal. Table 3 describes each step necessary to generate the LDMOS. Mesh density was varied in between process steps depending on areas of the structure that were being affected by the current process. These process steps were modified throughout the course of several simulations until an acceptable device was obtained. Once the proper fabrication conditions were determined, the FLOOPS structure served as the new baseline for subsequent design iterations. Figure 5 outlines this initial phase of the design, while Figure 6 shows one of the structures generated by FLOOPS.
Table 2

Fabrication Process Parameters for FLOOPS Simulator

<table>
<thead>
<tr>
<th>Process Commands</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Initialization</td>
<td>Material, Lattice Orientation, Spatial Coordinates, Resistivity</td>
</tr>
<tr>
<td>Mask</td>
<td>Left and Right Spatial Coordinates</td>
</tr>
<tr>
<td>Gas Flow</td>
<td>Gas Species, Pressure, Flow Rate</td>
</tr>
<tr>
<td>Implant</td>
<td><em>Mask</em>, Dopant Species, Dopant Dose, Implant Energy, Tilt, Rotation</td>
</tr>
<tr>
<td>Diffusion</td>
<td><em>Gas Flow</em>, Time, Temperature, Temperature Ramp Rate</td>
</tr>
<tr>
<td>Deposition</td>
<td>Material, Dopant Species, Dopant Concentration, <em>Diffusion</em>, Thickness, Isotropy</td>
</tr>
<tr>
<td>Etch</td>
<td>Material, Isotropy, Thickness, <em>Mask</em></td>
</tr>
</tbody>
</table>

Note: Italics indicate an inherited command
Table 3

LDMOS Fabrication Process

<table>
<thead>
<tr>
<th>Step</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Initialization</td>
<td>Low resistivity &lt;100&gt; p+ silicon substrate</td>
</tr>
<tr>
<td>2</td>
<td>Epitaxy</td>
<td>Lightly doped p- epitaxial layer. Thickness must support vertical component of SCR for given drain bias, but be lightly doped to allow low on-state channel resistance.</td>
</tr>
<tr>
<td>3</td>
<td>P-Body Implant</td>
<td>High dose implant to prevent source-side punch through and control threshold voltage. Rad-hard process prohibit self-aligned ion implantations through the gate oxide.</td>
</tr>
<tr>
<td>4</td>
<td>P-Body Drive</td>
<td>Can be adjusted together with implant mask to achieve optimal lateral diffusion underneath MOS gate.</td>
</tr>
<tr>
<td>5</td>
<td>Gate Oxidation</td>
<td>Thermal oxidation time, temperature and ambient are adjusted to produce desired oxide thickness.</td>
</tr>
<tr>
<td>6</td>
<td>Polysilicon Deposition</td>
<td>Adjusts the metal-semiconductor work function difference and provides low-resistance contact</td>
</tr>
<tr>
<td>7</td>
<td>Gate Stack Etch</td>
<td>Removal of thermal oxide and definition of the gate stack</td>
</tr>
<tr>
<td>8</td>
<td>LDD Implant</td>
<td>Energy and dose of the implant are adjusted to achieve optimal RESURF effect and low series resistance.</td>
</tr>
<tr>
<td>9</td>
<td>N+ Contact Implant</td>
<td>Forms low resistivity contact at silicon surface for source and drain metals</td>
</tr>
<tr>
<td>10</td>
<td>Source-Drain Anneal</td>
<td>Activates dopant species and repairs lattice damage from previous ion implantations</td>
</tr>
<tr>
<td>11</td>
<td>Contact Etch</td>
<td>Removal of thermal oxide to create contact window openings.</td>
</tr>
<tr>
<td>12</td>
<td>Finalization</td>
<td>Writes the completed structure to a DESSIS-compatible file format.</td>
</tr>
</tbody>
</table>
Figure 5: Establishment of Baseline Design
An LDMOS design generated by the FLOOPS fabrication simulator. Positive and negative doping concentration indicates donor and acceptor concentration respectively. FLOOPS generates a realistic device structure based on specified process conditions, including mask layer coordinates, dose and energy for ion implantations, and time, temperature and ambient conditions for thermal oxidation, implant drives, and anneal. Circuit simulations for FLOOPS structures can be performed using the DESSIS simulator.

Figure 6: FLOOPS-generated LDMOS Structure
3.2 Electrical Modeling

BV, $R_{DS-on}$ and $V_{th}$ were modeled using mixed-mode DESSIS simulations. In these types of simulations, the electrical state of the device structure is calculated at each mesh point using the previously mentioned semiconductor equations. During each solve iteration, parameters for each contact are saved. Among many others, these include carrier density, current, electric field, and potential. At the stopping point of the simulation, the state of the device is saved as a new structure file which can then be examined using TCAD.

Figure 7 shows the circuit used to model BV. The drain is reverse biased using a ramped DC voltage source in series with a large resistor. The gate and source are tied to a common ground. The DC voltage source is ramped iteratively until the drain current exceeds the stop condition for the simulation. Figure 8 shows a typical IV plot for the BV simulations. The plot shows an acceptable leakage current characteristic prior to avalanche breakdown. Figures 9 and 10 demonstrate the RESURF effect of the LDD. It can be seen from both figures that the electric field at avalanche is supported by a fully depleted LDD region. Once the LDD fully depletes, the electric field at the gate will increase. This continues until the field at the dielectric interface reaches the critical value for silicon.
Breakdown voltage plot generated by DESSIS, showing reverse leakage current and eventual breakdown at approximately 29 V. BV is defined at the point where the current slope approaches infinity.

Figure 7: Circuit Used to Model Breakdown Voltage

Figure 8: Typical IV Plot for BV Simulation
Electric Field at avalanche (top) and Doping Concentration (bottom). Note that the electric field is supported throughout the entire LDD region. Once the LDD becomes fully depleted, the electric field at the gate will begin to increase until it reaches a critical value. These results also show that a 2 μm epi layer thickness is sufficient to support the blocking voltage.

Figure 9: Electric Field at Avalanche Showing RESURF Effect
Electric field and electrostatic potential distributions at avalanche breakdown for the device shown in Figure 9. The plot (top) and structure (bottom) are aligned in the X dimension. The plot was taken from a Y-axis slice that passes just underneath the gate. Note that the peak electric field occurs at the gate after the LDD becomes fully depleted.

Figure 10: Electric Field and Potential Distributions at Avalanche Breakdown
Figure 11 shows the equivalent circuit for the $R_{DS-on}$ simulations. The drain bias is applied after the gate voltage reaches 4.5 V, and the simulation terminates when the drain current exceeds 5 $\mu$A/$\mu$m. The resulting IV plot is used to determine the resistance of the device in the on-state. The area specific on-resistance is then calculated by multiplying the slope of the IV plot by the device’s cell pitch and is expressed in units of $m\Omega\cdot mm^2$. As shown in Figure 12, the IV slope remains relatively linear throughout the range of applied drain voltages.

![Figure 11: Circuit Used to Model On-Resistance](image_url)
Figure 12: Typical IV Plot for On-Resistance Simulation

Figure 13 shows electron current distribution and the corresponding doping profile for a typical on-resistance simulation. The goal of the LDD design is to minimize the series resistance between the drain contact and the channel, while still supporting the required reverse voltage. In this case, the energy level of the LDD ion implantation was adjusted to situate the most highly doped region of the LDD as close as possible to the surface. The subsequent thermal drive forms a lightly doped diffusion region away from the surface and toward the blocking junction where it is best situated. Had the implant been deeper, a diffusion region would also have been formed adjacent to the channel, thereby increasing the series resistance unnecessarily.
Electron current density (top) and doping concentration (bottom). On-resistance is slightly improved by controlling the energy of the LDD implant to provide a highly conductive region near the top surface. In this case, there is no lightly doped “gap” between the channel and the most conductive region of the LDD.

Figure 13: Electron Current Density Distribution in the On-State
Figure 14 shows the equivalent circuit for the $V_{th}$ simulations. In this circuit, the gate and drain are tied to a ramped 5 V DC voltage source. The resulting IV plot shows drain current versus gate voltage. The threshold voltage can be measured one of two ways for the purposes of these simulations, as long as the same method is used consistently. The preferred method for experimental testing based on this type of plot is to extrapolate the linear portion of the increasing current back to a zero current level, as demonstrated in Figure 15. The intersecting gate voltage is $V_{th}$. The alternate method, suitable for modeling and design work, is to simply measure the gate voltage at a chosen current level for all devices.
The preferred method for experimental testing based on this type of plot is to extrapolate the linear portion of the increasing current back to a zero current level, as indicated by the dashed arrow. The intersecting gate voltage is $V_{th}$. The alternate method, acceptable for this work, is to simply measure the gate voltage at a chosen current level for all devices.

Figure 15: Typical IV Plot for Threshold Voltage Simulation
### 3.3 Design Optimization

Once a baseline fabrication process was created, a series of fabrication simulations and subsequent electrical modeling were conducted to optimize device performance. Separate groups of structures were dedicated to optimizing electrical performance by controlling three design parameters, namely the LDD dose, the P-Body dose, and the P-Body mask position. In each case, the design parameter was varied in both the positive and negative direction around the baseline structure. Each structure was then simulated using DESSIS to obtain BV, $R_{DS-on}$, and $V_{th}$ for each structure. This method not only provided a chance to find an improved design, but also served to validate the expectations described previously in Table 1.

The results of the DESSIS simulations on the resulting structures are presented in the following set of figures. The first set of simulations varied the LDD Implant dose while other parameters were kept constant. It was expected that on-resistance would be inversely related to the dose, and that threshold voltage would not be noticeably affected. Breakdown voltage should remain near constant as long as the LDD is fully depleted at breakdown. As the LDD implant dose is increased beyond a certain point, the RESURF effect is less than optimal, and the BV begins to fall. These conclusions are supported by the simulation results shown in Figures 16 and 17.
Variation in LDD implant dose generated the expected behavior. In each case, the resulting higher doping concentration from increased implant doses lowered series resistance. The BV remains high for low implant doses, because the LDD region is allowed to become fully depleted in those cases, thereby causing the BV to be determined solely by the distance between the drain and the gate. When the dose is increased beyond a certain point, the electric field builds up at the gate before the drift region becomes depleted.

Figure 16: Normalized LDD Dose versus BV and $R_{DS-on}$
Threshold voltage is determined primarily by the portion of the p-body implant that extends under the gate. Variations in LDD implant dose therefore have no effect on this parameter.

Figure 17: Normalized LDD Implant Dose versus Threshold Voltage

The next set of simulations varied the p-body implant dose while keeping other design parameters constant. It was expected that higher p-body doses would increase threshold voltage and on-resistance, as supported by the simulation results in Figure 18. The increased on-resistance occurs because a weaker inversion layer forms in a more highly doped p-type region for a given gate bias, meaning that a given gate voltage creates a less conductive channel. The increase in threshold voltage simply shows that a higher gate bias is necessary to invert more highly doped p-type silicon. The purpose of
simulating this effect is to determine what dose is necessary to achieve a threshold voltage closest to 2.5 V, as dictated by the design goal. The effect of the p-body implant dose on BV should be zero as long as the p-body region does not extend too close to the lightly-doped drain. This is supported by the data presented in Figure 19.

![Figure 18: Normalized P-Body Implant Dose versus $V_{th}$ and $R_{DS-on}$](image-url)
The final set of simulations show the effect of misalignment between the gate and the p-body. This is one of the most important parameters to consider for the rad-hard LDMOS, because threshold voltage adjustment cannot be accomplished using a self-aligned process, nor by an implant through the gate. The damage caused by an implant through the gate would create charge trapping vacancies within the dielectric, adversely affecting total-dose radiation hardness. Since neither technique is allowed, there is likely to be some misalignment between the p-body implant and gate masks. Therefore it is necessary to determine some range of tolerances for this misalignment.
The overlap between the p-body implant mask and the gate is noted as Lp#Lg. The following figures show the effect of varying this parameter around a safe baseline. Figure 20 shows that the p-body/gate overlap must remain within a narrow range to prevent an adverse effect on BV. If the overlap is made too large, then the drain/epi SCR will prematurely extend into the highly doped region of the p-body, and the electric field at the epi/p-body interface will reach a critical value before the LDD becomes fully depleted. If the overlap is made too small, then the drain/epi SCR will extend into the source/p-body SCR, resulting in punch-through and a very low BV. The “sweet spot” in terms of BV occurs when the drain/epi SCR does not extend into the highly doped region of the p-body at avalanche.

![Figure 20: Normalized P-Body/Gate Overlap versus BV](image)

Figure 20: Normalized P-Body/Gate Overlap versus BV
So long as there is sufficient misalignment between the p-body and gate to prevent punch-through, the main concern becomes the trade-off between threshold voltage and on-resistance. Figure 21 shows how the two are directly related. The increase in on-resistance is similar to the effect caused by increasing the p-body implant dose. Effectively, moving the p-body mask closer to the drain does increase the p-body dose, at least in the conductive channel region. The modeling served only to find a suitable tolerance for this design consideration.
The modeling data suggests that even a slight misalignment against the p-body implant can severely increase on-resistance. It is important to keep in mind that the severity of this effect is also dependent on the p-body implant dose and the time and temperature of subsequent thermal drives during fabrication. A lower p-body dose and/or a deeper drive could reduce the effect. However, one tradeoff to either technique might be reduced radiation hardness. Lowering the p-body doping concentration could make the device more vulnerable to threshold voltage shifts as trapped charge accumulates in the gate dielectric. This might not be a great concern, since the small gate area and inherently offers resistance to these effects. Another consideration is that increasing the resistance of the parasitic n-p-n base could make the device more susceptible to SEB. While the device is designed to collect hole current only at the bottom-side contact, significant hole current could be generated in this region in the event that the p-body itself is hit by a direct ion strike.
3.4 Mask Layout

The next phase of the design process is mask layout. The results of the modeling work were used to refine the baseline design for fabrication. It was decided to fabricate 20 full size LDMOSFETs with design parameters varied around the baseline. The length of the LDD region and the p-body/gate overlap were extended outside the scope of the modeling work, but remained centered around the baseline design. Nine devices were fabricated using a longer gate than was modeled. All of this was done on the assumption that the modeling data could be inaccurate.

In addition, a “pizza mask” was created utilizing the same silicon area as one of the large FET’s. This mask allowed for the creation of 18 additional designs on a much smaller scale. Seven small RESURF FET’s each consisting of a single unit-cell were fabricated on the pizza mask using alternate designs with exaggerated parameters. The 20 main designs were included in the pizza mask similarly. Seven self-aligned NMOS transistors were included, primarily for the purpose of threshold voltage measurements. Three RESURF diodes were designed to test the optimal BV of various LDD designs, and an n+/epi diode was designed to determine the BV of the source/epi junction without the RESURF effect. The use of a pizza mask is a common design practice. In the event that some problem prevents the large MOSFETs from functioning, the pizza mask could offer a chance to gain useful data from an otherwise failed run.
4 CHAPTER FOUR: EXPERIMENTAL RESULTS

Fabricated devices were tested in the UCF Power Semiconductor Research Lab using a Sony/Tektronix 370A programmable curve tracer connected to a wafer probe station. The probe station chuck was shorted to the source, and proper contact between the substrate and the chuck was tested before taking measurement. Two sets of measurements for BV, Vth, and IV characteristics were conducted for forty full-size devices on two selected wafers. Similar measurements were done for the smaller versions of those devices on the pizza mask. Typical results for functioning devices are shown in Figures 22-24.

Figure 22: Experimentally Obtained IV Plot
Threshold voltage measurement was done by applying $V_{DS} = 5$ V and then incrementally increasing the gate voltage until a specific level of drain current was reached. $V_{th}$ was measured at 250 $\mu$A for full-size devices and 5 $\mu$A for single unit-cell devices. Devices with the desired threshold voltage of $\sim 2.5$ V exhibited IV characteristics in which the drain current did not saturate. In general, threshold voltages for well-behaved devices were higher than desired – most near 4 V.
BV was measured by applying a zero gate bias and measuring $V_{DS}$ at $I_D = 25 \, \mu A$ for full-size devices and $I_D = 5 \, \mu A$ for small devices. Figure 24 indicates a BV near 26 V for the DUT. Breakdown voltages were generally higher than expected. Some non-functioning devices showed a BV exceeding 30 V, but failed to saturate in the on-state and/or had a very low threshold voltage. All of the well-behaved devices approached or exceeded the design goal of $BV = 25 \, V$. 

Figure 24: Breakdown Voltage Measurement
Table 4

Experimental Notes for One Wafer

<table>
<thead>
<tr>
<th>Gate Length</th>
<th>Lp/Lg (normalized)</th>
<th>Lhd (normalized)</th>
<th>Vth1 (V)</th>
<th>IV1</th>
<th>Vth2 (V)</th>
<th>IV2</th>
</tr>
</thead>
<tbody>
<tr>
<td>short</td>
<td>0.40</td>
<td>1.00</td>
<td>0</td>
<td>0</td>
<td>shorted</td>
<td>0.2</td>
</tr>
<tr>
<td>short</td>
<td>0.60</td>
<td>1.00</td>
<td>0.72</td>
<td>33.5</td>
<td>no saturation</td>
<td>4.67</td>
</tr>
<tr>
<td>short</td>
<td>0.90</td>
<td>1.00</td>
<td>2.72</td>
<td>31</td>
<td>no saturation</td>
<td>3.75</td>
</tr>
<tr>
<td>short</td>
<td>1.30</td>
<td>1.00</td>
<td>4.86</td>
<td>28</td>
<td>GOOD</td>
<td>4.4</td>
</tr>
<tr>
<td>short</td>
<td>0.60</td>
<td>0.79</td>
<td>0.51</td>
<td>28.4</td>
<td>no saturation</td>
<td>4.36</td>
</tr>
<tr>
<td>short</td>
<td>0.60</td>
<td>0.79</td>
<td>0.72</td>
<td>20.3</td>
<td>no saturation</td>
<td>2.36</td>
</tr>
<tr>
<td>short</td>
<td>0.60</td>
<td>0.79</td>
<td>0.71</td>
<td>21.3</td>
<td>no saturation</td>
<td>2.36</td>
</tr>
<tr>
<td>short</td>
<td>0.60</td>
<td>0.79</td>
<td>0.74</td>
<td>26</td>
<td>no saturation</td>
<td>2.36</td>
</tr>
<tr>
<td>short</td>
<td>0.60</td>
<td>0.79</td>
<td>0.74</td>
<td>26</td>
<td>no saturation</td>
<td>2.36</td>
</tr>
</tbody>
</table>

Table 4 shows the results of measurements on identical designs in two different mask fields on the same wafer. IV1 and IV2 indicate the general behavior of the IV characteristics. The most noticeable result from this and other similar sets of measurements was the wide variation in Vth for identical designs in different mask fields. Devices with very large p-body/gate overlaps consistently functioned best and showed consistently good yield. These measurements indicate misalignment between the p-body and poly-gate masks. It was later noted that both of those masks are aligned to a separate zero-level mask. This means that the range of likely misalignment between the p-body and poly-gate mask is doubled, since they are not aligned directly. BV was consistent...
throughout mask fields, indicating good alignment between the poly-gate and drain contact implant masks.

Total dose radiation testing was conducted at an outside facility shortly after fabrication. Measurements from those tests are not available at this time, but it was noted that the UCF LDMOS met or exceeded the tester’s standards for total dose hardness, including threshold voltage drift.
5 CHAPTER FIVE: SUMMARY AND FUTURE WORK

5.1 Future Work

The discrepancies between the modeling results and experimental results can be explained by conditions of the fabrication process that were not included in the modeling work. Some revisions will be proposed for the next fabrication run, both in mask layout and process flow. The most probable solution to the p-body misalignment issue is to set the p-body/gate overlap beyond the safe distance indicated by the functioning devices. The threshold voltage can then be reduced from 4 V to 2.5 V by reducing the p-body dose.

Some data such as on-resistance and gate charge have not yet been compiled, since those measurements are being conducted at an outside facility.

The most anticipated work at this moment is single event heavy ion testing, scheduled to take place in January 2008. This will be followed by extensive heavy ion modeling using DESSIS. Afterward a comparison of experimental and modeling data will be conducted to analyze the single event hardness of the LDMOS. Analysis of the single-event data will conclude the first phase of the LDMOS design cycle. An updated presentation of the results will be offered once that is complete.
5.2 Summary

In this paper, it is proposed that the LDMOS being developed at UCF is the next step in the advancement of radiation hardened power electronic devices. A description was offered of the destructive failure mechanisms associated with ionizing radiation exposure in state-of-the-art VDMOS power devices. It was shown through sound theory that the LDMOS might be inherently less vulnerable to those destructive effects. Further benefits of the LDMOS were described, including superior switching performance and reduced mass and cost. Based on these motivations, a 25 V hardened LDMOS was designed using TCAD software and fabricated in a CMOS foundry. Initial experimental results are promising in terms of both process viability and total dose radiation hardness. Experimental data will be available in the near future to show the single event radiation hardness of the UCF LDMOS.
LIST OF REFERENCES


