COPPER GALLIUM DISELENIDE SOLAR CELLS: PROCESSING, CHARACTERIZATION AND SIMULATION STUDIES

by

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I dedicate this research and this Dissertation to my Mom, Mrs. Arundhati Panse, and my Dad, Prof. Ramesh Panse. They both have played a major role in what I have accomplished in my life.
I am deeply indebted to Dr. Don Morel, my Major Professor. He guided and motivated me throughout this project, but his teachings went much beyond that. He always came across as a person of the highest integrity. He will always be a father figure to me.

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COPPER GALLIUM DISELENIDE SOLAR CELLS:
PROCESSING, CHARACTERIZATION AND SIMULATION STUDIES
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ABSTRACT

The goal of this research project was to contribute to the understanding of CuGaSe₂/CdS photovoltaic devices, and to improve the performance of these devices. The initial part of the research dealt with the optimization of a Sequential Deposition process for CuIn(Ga)Se₂ absorber formation. As an extension of this, a recipe (Type I Process) for CuGaSe₂ absorber layer fabrication was developed, and the deposition parameters were optimized. Electrical characterization of the thin films and completed devices was carried out using techniques such as Two-Probe and Three-Probe Current-Voltage, Capacitance-Frequency, Capacitance-Voltage, and Spectral Response measurements. Structural/chemical characterization was done using XRD and EDS analysis.

Current densities of up to 15.2 mA/cm², and Fill Factors of up to 58% were obtained using the Type I CuGaSe₂ Process. V₉₀C‘s, however, were limited to less than 700 mV. Several process variations, such as changes in the rate/order/temperature of depositions and changes in the thickness of layers, resulted in little improvement. With the aim of breaking through this V₀C performance ceiling, a new absorber recipe (Type II Process) was developed. V₀C‘s of up to 735 mV without annealing, and those of up to
775 mV after annealing, were observed. Fill Factors were comparable to those obtained with Type I Process, whereas the Current Densities were found to be reduced (typically, 10-12 mA/cm², with the best value of 12.6 mA/cm²). This performance of Type II devices was correlated to a better intermixing of the elements during the absorber formation.

To gain an understanding of the performance limitations, two simulation techniques, viz. SCAPS and AMPS, were used to model our devices. Several processing experiments and SCAPS modeling indicate that a defective interface between CuGaSe₂ and CdS, and perhaps a defective absorber layer, are the cause of the $V_{oc}$ limitation. AMPS simulation studies, on the other hand, suggest that the back contact is limiting the performance. Attempts to change the physical back contact, by changes in the absorber processing, were unsuccessful.

Processing experiments and simulations also suggest that the CuGaSe₂/CdS solar cell involves a true heterojunction between these two layers.
Photovoltaics is the method of converting sunlight into electricity. It is a simple and environmentally-friendly method of producing electricity. One promising way to make such solar electricity affordable for the layman is to use various thin film technologies such as Copper Indium Gallium Diselenide (CuIn(Ga)Se$_2$) and Cadmium Telluride (CdTe). Copper Gallium Diselenide (CuGaSe$_2$), which is a variation of CuIn(Ga)Se$_2$, has the potential to be used as a high-voltage-producing solar cell material, and, also, to be used as a material for multi-structured tandem solar cell systems. This document discusses the research project that focused on the development of a manufacturing-friendly process for making CuGaSe$_2$ solar cells, and the characterization, as well as the computer simulation studies of these solar cells.

The first chapter, Introduction, presents a detailed review of traditional (nonrenewable), as well as renewable electricity generation technologies. Although much of this chapter does not relate directly to the specific project undertaken during this research, it serves a dual purpose. First, it attempts to make a strong case (and, hopefully, succeeds in doing so) for the support of solar energy research. Secondly, it was deemed necessary, by the author of this document, to introduce the reader to the general topic of renewables. It is a need of the present time that every truly-concerned citizen not only take notice of renewables and their positive effect on the environment, but also recognize the responsibility to help bring about the transition to renewables from the traditional
non-renewable technologies. If the reader is already familiar with such topics, he or she should feel free to skip to the next chapter of this dissertation.

The second topic, Background, has two parts. Background I deals with the basic physics of solar cells. Background II reviews thin film photovoltaics in general, and then specializes into CuIn(Ga)Se$_2$ thin film photovoltaics. In addition to the treatment of fundamental workings of the relevant thin film devices, this chapter also provides historical perspectives, along with numerous references to the past research carried out in this area.

The third chapter introduces the reader to the fabrication, characterization and simulation techniques that have been used in this research endeavor. The next topic, Results and Discussion, has been divided into two parts. Part I deals with the processing and characterization results obtained with CuIn(Ga)Se$_2$ and CuGaSe$_2$, while Part II presents the computer simulation/modeling results.

Lastly, Chapter 6 presents our conclusions.
"We're altering the environment far faster than we can possibly predict the consequences. This is bound to lead to some surprises." --Dr. Stephen Schneider, National Center for Atmospheric Research.

1.1. Everything Under The Sun!

In our busy everyday routine, we hardly have the time and the willingness to stop and think about something as basic as Solar Energy. When we do (if we do), we often limit ourselves to thinking about the electricity generated using solar energy. And that’s only natural, because, in this hi-tech world that we are living, we are primarily concerned with only those things that can make our everyday life easier (and make ourselves lazier). The fact is that life on earth has always depended on solar energy. This was true before the invention of electricity, and is equally true now. Yes, of course, all of us have learnt, back in kindergarten, that the Sun is the star that gave birth to our mother Earth; that it was the solar energy that kept our planet warm enough so life could sustain here; and that without it, there would be no photosynthesis of the plants, and no light and warmth for the organisms to live and evolve. But who cares? We are here now, and the Sun’s here to stay (so we were told, at least). And we need our heater turned on because it’s too
darn cold, and the lights turned on because it’s kind of dark. And would you be kind enough to turn the TV on and pass me the remote please?

Well, maybe it’s a fact that we, in this modern commercialized world, have little time to think about anything outside the little circle that only contains our families, workplaces, and a few friends that our busy lifestyles can afford. Topics such as protecting the global environment of the very planet that we live on rarely attract our attentions anymore.

1.2. The Game of Power

Electric power has now become the fundamental platform that supports most of our physical needs. Indeed, it was only a couple of centuries ago that there was no electricity. But, today, it is so difficult to imagine ourselves without it. No wonder the California Power Crisis has scared many a folk, and is making the headlines at CNN everyday. Even scarier the fact is that there’s a possibility that the whole power situation is going to get a lot worse than it is now.

There are several factors that contribute towards the immense increase of electricity usage in the world seen in the recent times. Firstly, there’s the population growth. More people to use the power, so more power is needed. The birth of the official 6 billionth baby was recently celebrated. Official, because there are 250 babies born around the world in a single minute, and 15,020 in a single hour [http://www.census.gov]. The second-most important factor is the fast industrialization of the developing and underdeveloped countries. There are more factors, such as the
gradual spread of the (so-called modern) style of living, where larger joint families are often broken into smaller ones, so the houses and workplaces aren’t shared anymore, thereby increasing the total power usage.

As an example of how fast the demand for electricity is rising, in the United States alone, electricity sales increased by about 80% from 1975 to 1997 [Mcveigh, 2000].

Obviously, to keep up with this ever-increasing demand, the generation of electric power has to increase. Several technologies have been, and are being, used to generate this power. These can vaguely be divided into two types, traditional and non-traditional (renewable) technologies, and are reviewed below.

1.3. Traditional Electricity Generation Technologies

Traditionally, most of the electricity has been generated using the following three technologies:

(i) Power from Fossil Fuels: These fuels include oil, coal and natural gas,
(ii) Nuclear Power, and
(iii) Hydroelectric Power.

The first one, viz. fossil fuels technology, can be categorized as a non-renewable technology, meaning that the sources used for this technology cannot be recycled. The other two can be classified as renewables, and will be described in a later section. As of today, a majority (70%) of today’s power is, in fact, generated using fossil fuels [Sweet, 2001]. This is not at all surprising, for fossil fuels are abundant at present, and so the
resulting power is very cheap for the consumer. However, there are a few important aspects of this technology that show up as distinct disadvantages when we consider the future of electricity generation.

Firstly, although there seem to be enough coal and oil available right now, we know that the supply of these fuels cannot be infinite. While the demands shoot up, the fuels are gradually being depleted. There is going to be a time when this will start affecting the consumer’s wallet, and then there is going to be another time when there just are no more fossil fuels left that can be easily accessed by the humankind. There is disagreement among scientists and forecasters about when this might happen. According to some, it could be as early as the next decade, while others feel confident that newer fossil locations would be discovered that could delay this situation by decades, or even, centuries. Whichever direction one might choose to believe in, there can hardly be any disagreement about one thing: it is safer to find alternatives that can take up the burden of the fossil fuel technology, rather than to wait until the last minute.

Secondly, there are strong political implications of the fact that fossil fuel source locations are distributed unevenly around the world. One of the biggest proofs of this came about when the fossil fuel prices shot up in the wake of the Gulf War. Although such major events are rare, even minor uncertainties associated with the changes in international political relations that are results of internal policy changes of various countries, can have serious impact on the electricity bill that a consumer pays.

The third aspect is perhaps the most important one. There are serious environmental concerns associated with the use of fossil fuels as the source of electric power. These fuels -- coal, oil and natural gas -- were created chiefly by the decay of
plants that flourished millions of years ago. Burning these fuels unlocks the carbon stored by these plants and releases it to the air as carbon dioxide. For instance, burning one gallon of gasoline generates 22 pounds of carbon dioxide. In other words, it takes a pound of coal to generate the electricity to light a 100-watt bulb for 10 hours. For every pound of coal we burn, nearly three pounds of carbon dioxide go into the atmosphere. Since 1750, carbon dioxide in the air has risen by more than 30%. It could double by the year 2065! This atmospheric CO$_2$ rise over the years is depicted in the following figure.

![Image of CO$_2$ concentration over years]

**Figure 1.1. The Alarming Increase in the Concentration of Atmospheric CO$_2$**  
(Redrawn from [www.enviroweb.org](http://www.enviroweb.org))

Billions of tons of carbon dioxide are released into the atmosphere every year. This pollutes our atmosphere, but that is not where it stops. It is the cause of another permanent damage. The atmosphere has always contained carbon dioxide, methane and nitrous oxide. These gases, together with water vapor, trap some of the Sun's energy and keep the Earth warm enough to sustain life. This process is called the *Greenhouse Effect,*
which is a natural phenomenon. However, human activities increase some of the gases, and add new ones, thereby intensifying the natural greenhouse effect. This, according to many researchers, can eventually cause excessive warming of the atmosphere. Such a permanent change can potentially result in devastating effects such as the melting of polar ice, gigantic floods and rise of ocean levels.

Of course, there are skeptics that don’t yet believe in the greenhouse theory. However, in the words of James Hansen, Greenhouse Researcher, Goddard Institute for Space Studies, “It is time to stop waffling so much and say that the evidence is pretty strong that the greenhouse effect is here.”

Carbon dioxide accounts for three fourths of the predicted increase in the greenhouse effect. In addition to carbon dioxide, burning coal and other fossil fuels also releases sulfur dioxide, nitrogen oxides, and particulates, adding to the air-pollution.

One partial (and temporary) solution to this problem is to start using more natural gas, as natural gas releases lesser amounts of carbon dioxide. However, even these amounts are substantial, so alternatives to fossil fuels are deemed necessary. The so-called renewable technologies are the ideal alternatives. Let’s see why.

1.4. Renewable Electricity Generation Technologies

1.4.1. Survey

Let’s now take a look at the class of renewable technologies, two traditional ones of which are the nuclear power and the hydroelectric power.
The nuclear power alternative, although being used quite extensively, has drawn serious concerns regarding safety. Accidents such as at Chernobyl are still fresh in our minds. Moreover, the radioactive waste that is created in a nuclear plant has to go through an expensive and elaborate disposal. Such disposal practices have been proven to be quite controversial, and the public is becoming more and more aware of the uncertainties involved.

Hydroelectric power has also been developed extensively, taking up a major share of the electricity generation in developing countries. However, this, too, comes at the expense of the environment, essentially destroying the river ecosystems that the hydroelectric plants are built on. Therefore, significant expansion of this resource faces severe opposition from environmentalists. (An example of how this technology has had devastating effects on human life is the Narmada river/Sardar Lake project in central India: www.narmadabachao.com).

Because of the these reasons, although nuclear and hydroelectric are renewables, they cannot be considered exactly environment-friendly. This, then, leaves us with the five renewable technologies that can be considered environmentally clean, which are:

(i) Wind: Wind spins blades, which turn a generator to produce power.

(ii) Solar Photovoltaics (the topic of this dissertation): Sunlight is converted directly to electricity using appropriate semiconductor materials.

(iii) Solar thermal: Sunlight, reflected with the help of mirrors, is then used to boil water that runs a turbine to produce electricity.

(iv) Geothermal: Makes use of the natural heat present inside the earth. Steam coming up through wells is used to produce electricity.
(v) Biomass: Burning/extracting fuels from fast-growing plants produces power.

Because solar electricity is the topic of this research project, only this technology will be described in detail, and that is the subject of the next section.

1.4.2. Solar Energy Conversion

This energy is created by the fusion reactions that take place in the Sun, and is practically unlimited. The Earth receives about $7.45 \times 10^{17}$ kWh of this energy annually from the Sun in the form of sunlight. The annual power consumption of the world is approx. 400 Quadrillion BTU’s ($1.2 \times 10^{14}$ kWh). This means that if we have an economical and easy way of making use of the sunlight to produce electric power, our needs can be satisfied.

Ideally, a source of energy must be inexpensive, widely and easily available, easy to use, environmentally friendly and renewable. Solar energy satisfies most of these criteria. It’s free, environmentally clean and renewable. The only shortcoming is regarding the availability. There are some places around the world, which do not receive enough sunlight during a major part of the year. Obviously, solar energy would be a poor choice for such locations. However, even at the sunniest places, the sun is not available round the clock. (This drawback is also shared by the wind technology.) The result is an intermittent generation potential. Hence, it is vitally important that an appropriate storage technology such as hydroelectric pump storage or batteries to store electricity and/or potential energy is available. Otherwise, it may not be economical to employ this technology. It may, however, be viable to employ it as a secondary source to
complement an existing conventional electricity grid, provided the availability of the sun coincides with the periods of peak energy demand.

Photovoltaics is the process of conversion of solar energy into usable electric power. A typical photovoltaic cell is an integrated device consisting of layers of semiconductor materials and electric contacts. Several such cells are usually interconnected to form an integrated assembly that is called a solar cell module. Such modules are then placed at the appropriate places where they get exposure to bright sun. The absorption of this sunlight produces electricity, which can either be used directly, or, more often, is stored in some sort of energy-storage system for later use.

Today’s photovoltaic market is 151 Megawatts per year, corresponding to a value of about 0.7-1 billion US Dollars [Goetz]. Presently, there are about 34 photovoltaics module manufacturers in the U.S. [national center for photovoltaics, www.nrel.gov]. According to the Energy Information Administration [doe: www.eia.doe.gov], photovoltaic (PV) cells and modules shipments had reached about 50 peak megawatts in 1998. (Module shipments accounted for 32 peak megawatts, while cell shipments accounted for 18 peak megawatts.) Cells and modules that used crystalline silicon dominated the PV industry in 1998, accounting for 93 percent of total shipments, the remaining 7 percent of the share going to Thin-film technologies (to be explained later). In 1998, the average price for modules (dollars per peak watt) was about $3.94.

Although the solar power market growth in the last decade was between 15% and 20%, the consumption statistics indicate very clearly that solar technologies are not yet getting a major share of the energy production market. The reason is economical. The current cost of solar energy generation is about 30 cents per a kilowatt-hour (The current
cost of capacity, which is the capital cost measured by the dollar expenditure for the rated
capacity, is about $6000/kilowatt) [Mcveigh, 2000]. This cost of generation includes the
various costs at the point of production, such as those for the capital, the fuel, and the
operation and maintenance, and is then leveled with respect to the total costs of
production over the lifetime of the production facility. The cost, when compared with the
traditional electricity cost of about 6 to 8cents/kilowatt-hour, is still very high. However,
it is expected that, in the coming years, the cost of solar photovoltaics will continue to
decline. This feat can be accomplished by improving the conversion efficiencies of the
solar cells, while also improving the methods of capturing solar radiation.

1.4.3. The Past and Future of Renewables

In 1998, the renewable energy consumption in the United States was 7 quadrillion
Btu, accounting for almost 8 percent of the total U.S. energy consumption. The division
of total energy consumption into individual generation technologies for 1998 is depicted
in Figure 1.2 on the next page [Energy Information Administration: www.eia.doe.gov].
As can be seen from this figure, hydroelectric power and biomass dominated the
renewable energy market, with 50 percent and 43 percent shares, respectively. The
remaining 7% was split among solar, wind, and geothermal technologies. Table 1.1,
shown on the next page, contains information about U.S. renewable energy consumption
by energy source, for five years: 1994-1998. Note that this includes hydroelectric power,
and as can be seen from the numbers, increase in this power is mainly responsible for the
total renewable power increase from 1994 to 1998.
Figure 1.2. 1998 U.S. Energy Consumption by Energy Source

Table 1.1. U.S. Renewable Energy Consumption, in Quadrillion BTUs

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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Hydroelectric</td>
<td>2.971</td>
<td>3.474</td>
<td>3.913</td>
<td>3.922</td>
<td>3.540</td>
</tr>
<tr>
<td>Geothermal</td>
<td>0.395</td>
<td>0.339</td>
<td>0.352</td>
<td>0.328</td>
<td>0.334</td>
</tr>
<tr>
<td>Biomass</td>
<td>2.917</td>
<td>3.048</td>
<td>3.108</td>
<td>2.981</td>
<td>3.052</td>
</tr>
<tr>
<td>Solar</td>
<td>0.072</td>
<td>0.073</td>
<td>0.075</td>
<td>0.074</td>
<td>0.074</td>
</tr>
<tr>
<td>Wind</td>
<td>0.036</td>
<td>0.033</td>
<td>0.035</td>
<td>0.034</td>
<td>0.031</td>
</tr>
<tr>
<td>Total Renewable</td>
<td>6.390</td>
<td>6.968</td>
<td>7.483</td>
<td>7.339</td>
<td>7.032</td>
</tr>
</tbody>
</table>

According to the Electric Power Research Institute, today’s U.S. energy consumption by energy source is as shown below [Sweet, 2001].
It will be illuminating to compare today’s energy mix (Figure 1.3) to that of 1998. Several conclusions can be drawn from such a comparison.

Firstly, the proportion of fossil fuel power has decreased from 85% to 70%, which is a positive step towards reducing the devastating effects on the environment. However, inside of fossil fuels, the share taken up by natural gas has decreased, and this goes in the opposite direction, because natural gas is the least harmful than coal or oil. Similarly, although non-nuclear renewables’ (includes hydroelectric) percentage has increased from 8 to 12, the share of non-nuclear, non-hydroelectric renewables has actually gone down from about 4% to 2%.

Some of the renewable energy technologies have been in development for a few decades. In spite of this, renewables have failed to emerge as a prominent component of the energy generation, as can be seen from the above analysis. As mentioned before, the
main reason for this is the fact that the power obtained from these technologies is still expensive, when compared to that obtained from traditional generation technologies. It has hence been argued that renewables have not met the goals and claims that were set by their supporters. Mcveigh, et al. have addressed this issue in a recent publication [Mcveigh, 2000]. They have provided an evaluation of the performance of five renewable energy technologies, those being biomass, geothermal, solar photovoltaics, solar thermal and wind. Their findings refute the above argument. The authors conclude that renewable technologies have failed to meet expectations only with respect to market penetration. However, in terms of meeting the goals with respect to their cost, these technologies have succeeded, sometimes even exceeding those expectations.

An important thing to remember is that the main motivation for developing renewable energy technologies is the desire to get away from fossil fuels with their adverse effect on the environment. Use of such technologies will help both, to slow global warming, and to reduce air pollution. Traditional technologies may produce cheap power in terms of cost to the consumer. However, environmental, political, and health costs are not reflected in this cost. Were a cost assessed for the degradation of the environment and health, and were the other costs shifted from the taxpayer to the consumer, the increased cost would be significant [Gabor].

Tsur, et al. have used dynamic optimization methods to analyze the development of solar technologies in light of the increasing scarcity and environmental pollution associated with fossil fuel combustion [Tsur, 2000]. They have included shadow prices to account for this scarcity and pollution, to allow a valid evaluation of social costs and benefits of alternative energy options. Based on the analysis, the authors predict that
alternative energy sources will eventually capture an increasing share of energy supply. Moreover, their model “advocates substantial early engagement in solar R&D programs that should precede, rather than follow, future increases in the price of fossil fuels”.

Indeed, the only argument against the renewables is that these technologies are not cost-effective for the consumer. Here's an excerpt from Home Power Magazine, written by Randy Udall, explaining why we have to move past this "cost effective" argument: "Building 110 nuclear power plants before figuring out what to do with the waste is cost effective. Drowning the Columbia river and its priceless salmon runs is cost effective. Spending $50 billion a year to defend the Persian Gulf oil fields is prudent. Strip mining pays nice dividends: Wyoming coal is literally cheaper than dirt. Chernobyl was a superb investment. . . Conventional energy economics is a value system masquerading as mathematics. At its heart is one key assumption: the future is worthless and the environment doesn't matter. . . ”

Switching to renewables from the fossil fuels seems to be the only solution, when one considers the environmental factors. The advantages gained from such a switch are evident in the following example.

A one kilowatt PV system:
(i) Prevents 150 lbs. of coal from being mined,
(ii) Prevents 300 lbs. of CO₂ from entering the atmosphere,
(iii) Keeps 105 gallons of water from being consumed,
(iv) Keeps NO and SO₂ from being released into the environment,
each month! [www.solarenergy.org]
Unfortunately, because of the high retail cost, it is unfair to expect the consumer to opt for a solar panel rather than a connection to the conventional grid electricity. Therefore, there has to be an integrated effort from the layman, the Government and the Private Sector to make this switch from non-renewables to renewables possible. More public awareness will help build the public support, which hopefully will bring in the required change in the policies on the part of the Government. Recently, there has been a reduction in the amounts of Government funds for the development of such technologies as solar photovoltaics. Such policies have been, and are being, criticized both by technical and political supporters of photovoltaics. In Resources for the Future, John F. Ahearne writes about such issues [Ahearne, www.ulib.org]: “Although nuclear support (of the Government) has been productive, the large dollar amounts spent on such projects as the Clinch River Breeder Reactor could have been spent much better elsewhere. As far back as 1955, Greenewalt wrote, “I wonder what our position would have been today had the amounts of money and effort equivalent to those expended on atomic energy been devoted to the utilization of solar energy.” That same statement could have been made in 1965 and in 1975, and it can be made today.”

However, there is hope. The awareness about the environmental concerns is growing fast, thanks to various environmentalists’ groups and other non-profit organizations, and to the information technology. Even private sector companies seem to be taking notice. An example is the automotive industry. Most experts agree that within the next handful of years, consumers will see fuel-cell vehicles—100% clean engines that run on hydrogen and produce only water as a byproduct—hit the roads. [Why is BMW driving itself crazy?, Sue Zesiger, Fortune, 2000, www.fortune.com] In fact, a recent publication of possible energy scenarios up to the year 2060 predicts a multi-Gigawatt energy production by renewable technologies [Shell, 1997]. What then remains to be
seen is whether renewables will be used to their fullest potential, and whether they are able to replace the harmful fossil fuels in the near future. Because, in the words of Michael Oppenheimer, Senior Scientist of the Environmental Defense Fund:

"We have an obligation to weigh the risks of inaction against the cost of action. In that regard, global warming is no different than any other problem. But global warming is novel in one respect. It brings with it the possibility of a global disaster, and we have only one Earth to experiment on."
CHAPTER 2.
BACKGROUND I: BASIC PHYSICS

2.1. What’s a Solar Cell?

Photovoltaics (PV) is the conversion of light into electricity. When the source of light is the sun, the process is called Solar Photovoltaics (Although the “solar” part will be assumed hereafter). Because of the simplicity of this process, and the abundance of the source that it uses, it appears to be one of the most promising ways of meeting the increasing energy demands of our planet.

A solar cell, of the type that is used in this research, is essentially formed by sandwiching together a p-type semiconductor and an n-type semiconductor. Metallic contacts are made to both these semiconductors. The semiconductors are chosen in such a way that, when light is shone on the device, one of them will absorb a significant portion of the light. Absorption of the light creates mobile carriers, both negative (electrons) as well as positive (holes) in the material. Ordinarily, such generated carriers recombine in a semiconductor. However, a good solar cell is designed in such a way that most of these generated carriers, after they are swept across the junction, are collected by the metallic contacts. Such carriers are then made to flow in an external circuit, and their energy can be utilized. The phenomenon of solar energy conversion thus involves the processes of absorption of radiation, generation of carriers, transport of these carriers to the junction, separation of the carriers at the junction, collection of the separated carriers, and finally the utilization of the power generated.
A brief survey of the basic properties of p-n junctions, and the electronic processes involved when light interacts with a solar cell, is in order.

2.2. A P-N Junction in the Dark

An n-type semiconductor material has a large concentration of electrons, and a few holes, whereas a p-type semiconductor has a lot of holes, and a few electrons. When two such materials are appropriately joined together, diffusion of carriers takes place because of the large concentration gradients at the junction. Each electron leaving the n-side leaves behind an uncompensated positively charged donor ion, and every hole going across the junction leaves a negatively charged acceptor ion. These ionized donors and acceptors, present in the region depleted of carriers (called the depletion region $W$), build up an electric field. This field is set up such that it creates a drift component of current that opposes the diffusion of carriers. At thermodynamic equilibrium, when there is no net flow of charge across the junction, an equilibrium contact potential, also called a Built-in potential, $V_0$ is thus set up across the depletion region. This potential difference produces a bending of the energy bands of the semiconductors. Such a band bending is shown in the following figure, for the case of a homojunction p-n diode (made by using p- and n-doped parts of a single semiconductor).
When an external voltage is applied to the p-n junction diode shown above, one of two things can happen. If the bias is forward, i.e. a positive voltage $V_f$ is applied to the p-side, the height of the potential barrier is reduced from $V_0$ to $V_0 - V_f$, thereby reducing the band-bending. This increases the diffusion current of majority carrier electrons from the n-side surmounting the barrier to diffuse to the p-side, and holes surmounting their barrier from p to n. A large current, directed from the p- to the n-side, hence, flows in the
forward bias. On the other hand, if a reverse bias is applied to the junction (p-side negative with respect to the n-side), the bend-bending increases, and this decreases the diffusion current from p to n to negligible values.

The other current component that flows in a p-n junction is the so-called generation current, which is directed from n to p (opposite to the diffusion current). This is the drift component, composed of minority carriers from both the sides of the junction, and is relatively insensitive to the height of the potential barrier. These minority carriers are generated by thermal excitation of electron-hole pairs (EHP’s), at or near the junction, and are swept to the other side of the junction because of the electric field. In reverse bias, this is the only current present (because the diffusion current is negligible), and hence this current component is sometimes referred to as the reverse saturation current, $I_0$, with the corresponding current density denoted by $J_0$. Note that the letters $I$ and $J$, hereafter, will refer to the currents and the corresponding current densities. The total current density in a p-n junction in the dark can be written as:

$$J = J_0 \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]$$  \hspace{1cm} (Eq. 2.1)

Where the $J$ and $J_0$ designate the total and the reverse current densities, respectively, $V$ is the applied voltage, $k$ is the Boltzmann constant, $q$ is the electronic charge, and $T$ is the absolute temperature. As can be easily seen, at equilibrium ($V = 0$), the net current is zero. The above equation defines the I-V characteristic of the junction diode, which is shown graphically in the next section.
2.3. Interaction with Light

2.3.1. Photocurrent

When light is shone on the junction, the photons that have energies greater than the bandgap of the semiconductor have a high probability of being absorbed. The absorption of light can be described by relating the radiation intensity $I_0$ falling on a semiconductor surface to the intensity $I$ that remains after the light has penetrated a distance $x$:

$$I(\lambda) = I_0 \exp[-\alpha(\lambda)x] \quad \text{(Eq. 2.2)}$$

The parameter $\alpha$, which is a function of the wavelength of the light, is a characteristic of the material, and is called as the absorption coefficient. The value of the absorption coefficient must be high for the absorber material used in a solar cell device, so that most of the light is absorbed in a useful way.

Each photon that is absorbed in the absorber material generates an EHP. Such minority carriers, if generated within a certain distance of the junction (called a diffusion length), can diffuse to the junction, be swept to the other side, and be collected by appropriate contacts.

When a monochromatic light of wavelength $\lambda$ is incident on the surface of a solar cell, the photocurrent and spectral response, that is, the number of carriers collected per incident photon at each wavelength, can be derived as follows [Sze, 1981].

The generation rate of electron-hole pairs at a distance $x$ from the semiconductor surface is given by:
\[ G(\lambda, x) = \alpha(\lambda) F(\lambda)[1 - R(\lambda)] \exp[-\alpha(\lambda)x] \]  
(Eq. 2.3)

Where \( F(\lambda) \) is the number of incident photons per \( \text{cm}^2 \) per unit bandwidth, and \( R(\lambda) \) the fraction of these photons reflected from the surface. Using the appropriate boundary conditions, and assuming low-injection conditions, the internal spectral response (SR) is given by

\[ SR(\lambda) = \frac{1}{qF(\lambda)[1 - R(\lambda)]} \left[ J_p(\lambda) + J_n(\lambda) + J_{dr}(\lambda) \right] \]  
(Eq. 2.4)

Where \( J_p(\lambda), J_n(\lambda), \) and \( J_{dr}(\lambda) \) are the photocurrent contributions from the p-region, the n-region, and the depletion region, respectively.

Once the SR is known, the total photocurrent density obtained from the solar spectrum distribution \( F(\lambda) \) is given by

\[ J_L = q \int_0^{\lambda_e} F(\lambda)[1 - R(\lambda)]SR(\lambda) d\lambda. \]  
(Eq. 2.5)

The generation of EHPs because of light gives rise to an added generation rate \( g_{op} \), given in \( \text{EHP/cm}^3\cdot\text{s} \), which produces a current from the n- to the p-side (opposite to the dark forward diffusion current). If \( L_p \) and \( L_N \) are the diffusion lengths for the minority carrier holes and electrons, respectively, then the resulting optically generated current for a junction of area \( A \) \( \text{cm}^2 \) and depletion region width \( w \) can be written as:

\[ J_L = qAg_{op}(L_p + L_N + w) \]  
(Eq. 2.6)

Figure 2.2 depicts the current generation in the p-n junction under illumination. Since this current is from n to p, it subtracts from the total current from p to n.
2.3.2. I-V Characteristics

The resulting I-V characteristic of the diode, in dark as well as in light, is shown in the following figure.

Figure 2.3. I-V Characteristic of an Ideal p-n Junction Solar Cell
Depending upon the intended application, the diode can be operated either in the third or the fourth quadrants of the I-V characteristic. Power is delivered to the device from the external circuit when the current and junction voltage are both positive or both negative. If operated in the fourth quadrant, however, power is delivered from the junction to the external circuit, and this is the principle of operation of a solar cell device.

The next figure shows an equivalent circuit of a solar cell. The generation of the photocurrent $I_L$ is represented by a current generator, in parallel with a diode that represents the p-n junction.

\[ I_L, \quad I_D, \quad R_S, \quad R_P \]

**Figure 2.4. An Equivalent Circuit of a Solar Cell**

There are two resistances shown in the above figure. $R_S$ is the series resistance, which should ideally be zero, but always exists, in a practical solar cell. It involves the bulk resistance of the absorber semiconductor, as well as any other resistances in the device such as those coming from the contact materials used.

The parallel (or shunt) resistance $R_P$ represents any parallel paths for the junction current to flow (an example is metal particulates shunting the junction). Ideally, such parallel paths shouldn’t exist, making $R_P$ infinite.
For simplicity, let us assume that the current generated by light can be added to the current flowing in the dark (superposition), and also that $R_S = 0$, and $R_P = \infty$ (ideal case). Then, the current density $J$ flowing in the device in the presence of light can be expressed as:

$$\begin{align*}
J &= J_0 \left[ \exp \left( \frac{qV}{AKT} \right) - 1 \right] - J_L \\
\text{(Eq. 2.7)}
\end{align*}$$

Here, the first term on the right is the forward current driven by the voltage $V$, and the second term is the (reverse) light generated counterpart. $J_0$ is often referred to as the reverse saturation current.

A few important terms that are commonly used as measures of solar cell performance need to be defined. The short-circuit current density $J_{SC}$ is simply the light generated current $J_L$. The open-circuit voltage can be obtained by setting $J = 0$.

$$\begin{align*}
J_{SC} &= J_L \\
\text{(Eq. 2.8)}
\end{align*}$$

$$\begin{align*}
V_{OC} &= \frac{kT}{q} \ln \left( \frac{J_L}{J_0} + 1 \right) \\
\text{(Eq. 2.9)}
\end{align*}$$

It can be easily seen that, while the $J_{SC}$ depends only on the light-assisted generation, the $V_{OC}$ depends on the current generation-recombination processes as well as on the nature of the junction transport ($A$ and $J_0$). Both $I_{SC}$ and $V_{OC}$ are shown in the I-V characteristic above.

No power can be generated under short or open circuit. The maximum power $P_{MAX}$ produced by a device is reached at a point on the characteristic where the product
IV is maximum, that is, when the area covered by the power rectangle shown in the
figure is maximum. The Fill Factor (ff) is defined as:

$$FillFactor(\text{ff}) = \frac{I_{\text{MAX}}V_{\text{MAX}}}{I_{\text{OSC}}V_{\text{OC}}}$$  \hspace{1cm} (Eq. 2.10)

The FF, therefore, is a measure of the squareness of the characteristic. The efficiency $\eta$
of a solar cell is defined as:

$$\eta = \frac{P_{\text{MAX}}}{P_{\text{RAD}}}$$  \hspace{1cm} (Eq. 2.11)

Which, in terms of $V_{\text{OC}}$, $J_{\text{SC}}$ and FF, becomes:

$$\eta = \frac{J_{\text{SC}}V_{\text{OC}} \text{ ff}}{P_{\text{RAD}}}$$  \hspace{1cm} (Eq. 2.12)

Where $P_{\text{RAD}}$ is the power of the radiation incident upon the cell. The standard conditions
used to calculate the solar cell efficiency are: an irradiance of 100mW/cm$^2$, standard
reference AM1.5 spectrum, and a temperature of 25\(^0\)C.

When we consider a practical solar cell, the above equation for the current
transport has to be modified. Real cells usually have a non-zero series resistance $R_s$, and
a finite shunt resistance $R_P$. The equation for the current $I \ (= J \times \text{Area})$ then becomes:

$$I = I_0 \left\{ \exp\left[\frac{q(V-IR_s)}{AkT}\right] - 1 \right\} + \frac{(V-IR_s)}{R_P}$$  \hspace{1cm} (Eq. 2.13)
The factor $A$, in the denominator of the exponential, is the so-called *ideality factor*, which relates to the mechanism of the junction transport in a practical device. The value of $A$ usually varies between 1 and 2. A value of 1 usually means that the junction transport is by diffusion, whereas a value of 2 signifies that the transport is controlled by recombination in the depletion region.

If the values of $R_S$ and $1/R_P$ are significant, then the I-V characteristic of the device gets affected, as shown in the next two figures. To the first order, $V_{OC}$ is unchanged by a reasonably low $R_S$, whereas $I_{SC}$ decreases slightly. On the other hand, a finite $R_P$ usually decreases $V_{OC}$, while $I_{SC}$ is unaffected.

![Figure 2.5. Effect of a Non-Zero Series Resistance on the I-V Characteristic](image)

Figure 2.5. Effect of a Non-Zero Series Resistance on the I-V Characteristic
Figure 2.6. Effect of a Finite Shunt Resistance on the I-V Characteristic

The most common types of junction that are used to form solar cells are:

(i) Homojunction: p-n junction within the same semiconductor material.

(ii) Heteroface structure: similar to a homojunction, but with an added window layer made of a larger band-gap semiconductor.

(iii) Heterojunction: p-n junction between two different semiconductor materials.

(iv) Schottky barrier: metal-semiconductor junction.

2.4. Heterojunctions

When semiconductors of different bandgaps and electron affinities are brought together to form a junction, as in a heterojunction, discontinuities are produced in the
energy bands, as the Fermi level of the different materials line up at equilibrium. The discontinuities in the valence ($\Delta E_V$) and the conduction bands ($\Delta E_C$) accommodate the difference in the bandgaps. Figure 2.7 (on the next page) shows an example of such a heterojunction system, and the important parameters, before the two semiconductors are joined together. The band bending that occurs after the two are joined together is depicted in Figure 2.8.

It can be seen, from the resulting band-bending, that a spike has appeared in the conduction band, where the two materials meet. Such a spike is the result of properties specific to the materials used, such as the electron affinities $\chi$'s. A discontinuity such as this limits the electron current that flows from the p-side to the n-side when the solar cell is placed in the light, and hence should be avoided by proper selection of the semiconductor materials, and by appropriate processing.

![Figure 2.7. Two Materials, Before Heterojunction Formation](image)

31
Figure 2.8. Heterojunction Formation

It should be noted that, in heterojunctions, the light can either be incident on the larger band-gap material (backwall-type) or on a thin layer of the smaller band-gap material (frontwall type). Similarly, in Schottky barriers, it is possible to have the light incident on either the semitransparent metal forming the barrier (frontwall), or through the semiconductor (backwall) [Bube].
The solar cells that are the topic of this research can be considered to be backwall-type heterojunction solar cells. A heterojunction can be either isotype, where both the semiconductors have the same type of conductivity, or anisotype, where the conductivities are different. Again, the CuGaSe$_2$/CdS junction used in this research belongs to the latter type, viz. anisotype.

The principle advantage of using a direct bandgap heterojunction system for a solar cell, such as the one used in this research can be seen as follows. Consider the case of an indirect bandgap homojunction solar cell, an example of which is a Silicon solar cell. Here, because of the low absorption coefficient associated with the indirect bandgap, a large thickness of the material is needed to absorb enough light. If we consider replacing this system by a direct bandgap homojunction system, another problem arises. Because the light needs to be absorbed as close to the junction as possible (so that the generated carriers are easily collected by the junction), the top layer (say, n-layer) needs to be fairly thin, with a thicker p-layer underneath it. In such a structure, the carriers generated in the n-layer have a high probability of diffusing away from the junction, towards the front contact, and eventually getting lost because of the high surface recombination velocity at the contact surface. Now, if the system is a direct bandgap heterojunction, then it can be designed in such a way that the top n-layer is made of a wider bandgap material which will absorb little light in the spectrum of interest. Most of the light hence will reach the junction and the underlying p-type absorber, thereby significantly reducing the likeliness of surface recombination at the front contact. The p-CuIn(Ga)Se$_2$/n-CdS solar cell structure has been optimized in this way, and the resulting band diagram is shown below, along with the n-type ZnO which acts as the
front contact. The CuGaSe$_2$/CdS cell has a very similar structure, except that the conduction band of the absorber is raised further above, a direct effect higher bandgap of CuGaSe$_2$.

![Band Diagram of the CuIn(Ga)Se$_2$/CdS/ZnO Solar Cell](image)

**Figure 2.9. Band Diagram of the CuIn(Ga)Se$_2$/CdS/ZnO Solar Cell**

For heterojunction solar cell structures, an added complication is the increased defect states at the interface. These mainly arise because of the lattice mismatch between the two semiconductors. However, processing conditions may also have a strong effect. Therefore, unlike in homojunctions, the carrier transport properties in heterojunctions are usually dominated by phenomena in the interface region. The current transport in the
depletion layer has been attributed to either the recombination, or the tunneling, or a combination of both. This transport is aided by the defect energy levels at or near the interface. A large density of electrically active interface states provides two mechanisms: (i) The charge stored in these states distorts the band profile, and (ii) The states give rise to a high density of recombination centers, thereby producing high forward current ($J_0$) values.

In some cases, the extremely high density of charged states at specific energy levels at the interface is sufficient to pin the surface (or interface) Fermi level at that energy.
3.1. Historical Background of Photovoltaics

Becquerel reported the photovoltaic effect in 1839, when he found that a light-dependent voltage developed between electrodes immersed in an electrolyte. In 1876, this effect was observed in an all-solid-state Selenium system. Subsequent work on the PV effects in selenium and cuprous oxide led to the development of the selenium PV cell that was widely used in photographic exposure meters. The modern era of PV began in 1954, when Chapin et al., at the Bell laboratories, successfully developed a silicon single-crystal solar cell. This device represented a major development because it was the first photovoltaic structure that converted light to electricity with a reasonable efficiency (6%).

Until the 1960’s, the main interest in the development of solar cells was their application as power sources in spacecraft. The early 1970’s saw a growing interest in the development of PV technologies for terrestrial use. More recently, the focus has shifted from single-crystal technology to the low-cost alternative of thin film technology.

Before going into the specifics of PV technologies, it will be worthwhile to outline the general requirements for such a technology. The most important of these are listed below.
(i) Conversion efficiency should be high for laboratory cells as well as for modules. (As the cost decreases, this requirement becomes less important. However, realistically, to keep the area-related costs down, module level efficiencies of at least 10% are necessary.)

(ii) Constituent materials (semiconductors, metals) should be readily available, and should be inexpensive.

(iii) A simple but reproducible deposition method that is suitable for large area production should be available.

(iv) The cells/modules must be stable over long periods of time.

(v) Total (capital + maintenance) cost should be low.

(vi) Constituent materials should be non-toxic/environmentally friendly.

Currently, the most widely used PV technologies are the single-crystal silicon technology and the polycrystalline silicon technology. Together, these two forms of silicon constitute about 86% of the solar cell market today [Goetzberger]. However, there are distinct disadvantages of using silicon as the absorber material for solar cells, as described below.

Silicon is an indirect bandgap semiconductor, with a relatively low absorption coefficient for absorbing sunlight. Consequently, a considerable thickness (about a 100 microns) of silicon is needed to absorb the light, thereby increasing the material cost. This, in turn, means that the photogenerated carriers have to traverse long distances to reach the junction, which is near the front surface. The diffusion length of the minority carriers has to be very high, which can happen only when the material is of very high purity and of high crystalline perfection. This, then, increases the processing costs.
Moreover, the single-crystal or polycrystalline silicon wafers are cut from ingots grown by the Czochralski method, or by controlled solidification in a crucible or mold. Sawing of these wafers results in material loss, adding to the total material cost.

Although the laboratory efficiencies of these cells have exceeded 24%, the commercially available module efficiencies are usually limited to less than 16%. It is surprising that, in spite of these shortcomings, silicon is the dominant solar cell technology. At least a major part of the reason lies with the fact that this technology has benefited tremendously from the high standard of silicon technology that was originally developed for transistors, and later for integrated circuits. The resulting silicon-based solar cells have exhibited high efficiency and good stability. The best laboratory efficiency for a single-crystal silicon solar cell is 24.5% [Green, 1999], while the best production cells have efficiencies of 15-16%. However, the resulting electricity costs are still relatively high, when compared to the cost of conventional electricity, making it necessary to look for new materials and technologies to replace silicon.

One alternative to the silicon technology that has been extensively investigated is the gallium arsenide (GaAs) technology. GaAs is a direct bandgap semiconductor with a high absorption coefficient, with the bandgap of 1.43 eV that is well suited to the solar spectrum. The effect of the direct bandgap is easily appreciated when it is recognized that, for a 90% light absorption, it takes only 1 µm of GaAs, versus 100 µm of silicon. This technology, however, is quite expensive, and, as a result, more and more scientists and researchers are getting interested in the development of the low-cost alternative, viz. thin film photovoltaics.
3.2. Thin Film Photovoltaics

The three thin film technologies that hold the greatest promise are: Amorphous Silicon (a-Si), Cadmium Telluride (CdTe) and Copper Indium Diselenide (CuInSe$_2$).

The a-Si technology, which uses a silicon-hydrogen alloy (containing 20-30% hydrogen) as the absorber material, has been around for a couple of decades. The first amorphous solar cells were prepared in 1976 [Carlson, 1976]. The a-Si technology currently dominates the thin film photovoltaics market. (The dominance of silicon in its crystalline and amorphous forms is an overwhelming 99% of the total photovoltaics market. Most of the remaining 1% is taken up by CdTe, with CuInSe$_2$ only recently beginning to show up on the commercial scene.)

The cuprous sulfide/cadmium sulfide heterojunction was the first all-thin-film photovoltaic system developed. Currently, two of the most promising thin film polycrystalline technologies are Cadmium Telluride (CdTe) and Copper Indium Diselenide (CuInSe$_2$), both of which use Cadmium Sulfide (CdS) as the (n-type) heterojunction partner. Both CuInSe$_2$ as well as CdTe are direct bandgap materials. Such polycrystalline thin film PV technologies offer several advantages, which can be weighed against the shortcomings of single-crystal and poly silicon cells that are listed above. These are:

(i) Thin film technologies often involve semiconductor materials that have direct bandgaps, and hence have very high absorption coefficients for the wavelengths of interest. Therefore, only a small thickness, usually a few
micrometers, is enough to absorb all of the sunlight incident on the absorber layer. This provides for significant savings in the material costs.

(ii) Because of the low consumption of the active solar cell material, rare and expensive materials can be considered.

(iii) A variety of relatively inexpensive vacuum deposition techniques can be employed for the processing of thin film solar cells, thereby reducing the processing costs. These techniques include RF and DC magnetron sputtering, vacuum evaporation, close-space sublimation, etc.

(iv) There are no small wafers to wire together, while making solar cell modules. Separate cells can be monolithically integrated on the module by scribing steps between depositions [Gabor, 1995]. This makes packaging and wiring easier, and also allows high voltage to be produced with smaller areas [Goetzberger].

(v) Thin films can be deposited on flexible, lightweight substrates, thereby making the cells viable for a larger variety of applications.

Based on this list of desirable properties, one might begin to think that thin film technologies are clearly the one solution that will get rid of all the hurdles that PV faces. However, in spite of all these advantages, these technologies haven’t been able to get the electricity cost down enough, thanks to the following shortcomings.

(i) Most of the thin film technologies involve heterojunctions, and hence face the problem of faulty interfaces, arising because of lattice mismatches between the materials.

(ii) Difficulty of getting different films to adhere to each other well.
(iii) Difficulty in achieving uniformity of thickness, composition, and quality across a large substrate.

(iv) Difficulty in achieving stability of the films over many years.

(v) Toxicity of some constituents involved (for instance, Cd in the case of CdTe/CdS, and, to a lesser extent, CuInSe₂/CdS).

Although thin film PV technology is still in its infancy, both CdTe as well as CuInSe₂ technologies have shown tremendous promise. Laboratory efficiency numbers have exceeded 18% for CuIn(Ga)Se₂, and 15% for CdTe, whereas commercially available thin film modules have shown conversion efficiencies in the neighborhood of 10-12%.

One of the main problems facing the CdTe technology is the toxicity of cadmium. This necessitates end-of-life recycling programs for CdTe modules, thus adding to the total cost. CuInSe₂, on the other hand, has consistently passed the toxicity tests, and hence can be thought of as the leader among all current thin film technologies.

3.3. CuInSe₂-Family-Based Thin Film Photovoltaics

3.3.1. CuInSe₂ Family and Device Issues

The CuInSe₂-family of thin films belongs to the I-III-VI class of thin film semiconductors, and has shown great promise for photovoltaic applications. With a direct bandgap of 1.0 eV, CuInSe₂ has the highest reported absorption coefficient of
about $3.6 \times 10^5$ cm$^{-1}$. The CuInSe$_2$ family includes several I-III-VI compounds, which will be described in the next section.

The typical structure of a completed solar cell device based on the CuInSe$_2$ absorber material would be: Glass substrate/ Molybdenum / CuInSe$_2$/ CdS/ Zinc Oxide. Here, the junction is essentially formed between the p-type CuInSe$_2$ and the n-type CdS. The molybdenum and zinc oxide thin films are used as the back contact and the front contact, respectively. The light is incident from the front (zinc oxide) side.

CuInSe$_2$ is a I-III-VI ternary (i.e., three elements) compound. The following figure shows the so-called chalcopyrite structure of this compound, which, essentially, is a diamond-like lattice made up of face-centered tetragonal unit cells.

![Figure 3.1. The CuInSe$_2$ Structure [Zhang, 1998]](image)
CuInSe$_2$ is a self-doped (intrinsically doped) material, which means that, when the compound is formed, it automatically becomes either p- or n-type, depending upon the composition. The primary intrinsic defects, which are also called native defects, include copper vacancies (V$_{\text{Cu}}$), copper-on-indium (Cu$_{\text{In}}$) antisites, indium-on-copper antisites (In$_{\text{Cu}}$), and selenium vacancies (V$_{\text{Se}}$). The former two produce acceptor type defects, whereas the latter two give rise to donor-type defects. Depending upon the ratio of the Group I to Group III (commonly referred to as the metal ratio), the CuInSe$_2$ material can be made either Cu-rich or In-rich. Cu-rich material is highly conductive, mainly because of the presence of unreacted, and highly conductive, copper selenide species. This material is generally p-type, due to a large concentration of Cu$_{\text{In}}$ defects. The performance of the solar cells that have Cu-rich absorber layers is usually diminished. This has been attributed to the above-mentioned copper selenide forming between the grain boundaries, thereby shorting the p-n junction. The In-rich CuInSe$_2$ material, on the other hand, does not contain copper selenide species. This type of material can be either n- or p-type. Usually, the In$_{\text{Cu}}$ donor defects and the V$_{\text{Cu}}$ acceptor defects are present in this material at the same time, reducing the conductivity of the layer (the so-called compensation effect). The efficient self-doping ability of CuInSe$_2$ has been attributed to the exceptionally low formation energy of Cu vacancies and to the existence of a shallow Cu vacancy acceptor level [Zhang, 1998].

In general, there are two methods that have primarily been used to carry out the vacuum physical vapor deposition of CuInSe$_2$ absorber films. One predominant method is the simultaneous co-evaporation of all the elements onto the substrate material. High quality thin films can be obtained by this technique. In fact, the best CuInSe$_2$ device
reported in the literature has been fabricated at NREL using a three-stage co-evaporation approach. After an anti-reflective coating, the device parameters reported were the following: Area = 0.395cm$^2$, $\eta = 13.2\%$, $V_{OC} = 484$ mV, $J_{SC} = 36.29$ mA/cm$^2$, and FF = 75.10\% [Contreras, 1994]. A small area of co-evaporated CuInSe$_2$ thin films was reported to have an efficiency of more than 15\% [Tuttle, 1996]. There are, however, some disadvantages of the co-evaporation technique. Firstly, the technique requires a very high control of deposition parameters, especially because three, or sometimes even four, elements are being deposited at the same time. Secondly, evaporation, by its very nature, is an expensive process, in terms of material usage. Thirdly, large-area uniform depositions are difficult to achieve with evaporation (compared to, say, sputtering). This, therefore, makes it difficult to scale this method for a high-volume commercial production.

The other approach that is being explored for the formation of the CuInSe$_2$-type absorbers usually includes two steps. The first step involves the deposition of the so-called precursors, which essentially are alloys of copper and indium (and sometimes gallium), by a physical vapor deposition technique such as evaporation or sputtering. In the second high-temperature step, commonly referred to as selenization, the precursor films are exposed to a high flux of selenium-containing vapors, by using either elemental selenium, or a selenium compound such as hydrogen selenide (H$_2$Se). With this method, it is sometimes difficult to achieve a highly homogeneous absorber film. Although high-efficiency solar cells have been fabricated using this method, the performance is usually inferior to that obtained by the co-evaporation technique.
In a recent paper, Kim, et al. reported a study of the CuInSe$_2$ selenization parameters [Kim, 2000]. The CuInSe$_2$ absorber was prepared using a two-step method. To accomplish a homogeneous precursor layer, they used DC magnetron co-sputtering from a Cu-In alloy. Only two phases, Cu$_{11}$In$_9$ and CuIn$_2$, were formed over a wide range of compositions, suggesting that a high degree of elemental mixing occurred. (Others have reported existence of other phases, such as Cu and Cu$_{1n}$, in sputtered or evaporated bi-layer or multi-layer Cu-In precursor films.) The selenization of the precursors involved two stages. In the first stage, selenium was incorporated into the alloy precursor film at a lower temperature of 250$^\circ$C. The second stage involved a re-crystallization process, which was performed at an elevated temperature of 400-550$^\circ$C. The authors then compared selenization at two different pressures: 10mTorr vacuum, and 1atm. At atmospheric pressure, the scattering because of the Argon present in the system reduced the energy of the Se atoms. These low-energy atoms induced localized reactions, resulting in several intermediate compounds. In vacuum, on the other hand, the Se atoms had higher energy, and could migrate easily on the surface to promote a reaction with the metals. This indicated that the formation of CuInSe$_2$ single phase needed higher temperature treatment to obtain enough Se energy.

Several recent studies have identified the presence of a thin (a few hundred angstroms) n-type layer at the surface of the CuInSe$_2$ absorber films. Such layers have been referred to as ordered vacancy compounds (OVC’s), ordered defect compounds (ODC’s) or chalcopyrite defect compounds (CDC’s). The improved CuInSe$_2$ device performance has been attributed to these defect layers. Abulfotuh, et al. characterized CuInSe$_2$ layers using photoluminescence, and detected the presence of a 250$\AA$ thick In-
rich defect layer. They also found that this layer, which was previously identified as CuIn$_3$Se$_5$, had a gradual change of composition (Cu content) with depth, which resulted in a gradual change in the optical properties of the films [Abulfotuh, 1996]. Later, Zhang, et al. showed that the ODC’s in CuInSe$_2$ resulted from the unusual stability of a special defect pair: (In$_{Cu}^{2+} + 2V_{Cu}^{-}$), i.e., two Cu vacancies next to an In-on-Cu antisite. Evidently, a periodic spatial repetition of this pair gives the ODC’s [Zhang, 1998]. The electrically benign character of the large defect population in CuInSe$_2$ has also been explained in terms of an electronic passivation of the In$_{Cu}^{2+}$ by the 2$V_{Cu}^{-}$. Such a special defect pair can be seen in the following figure.

Figure 3.2. The Structure of a Special Defect Pair [Zhang, 1998]
3.3.2. Bandgap Engineering

The open circuit voltage produced by a solar cell is proportional to the band-bending that is produced at the junction where the p- and n-layers meet. This band-bending, in turn, increases as the bandgap of the absorber layer increases. However, such an increase in $V_{OC}$, with an increase in the absorber bandgap, comes at the cost of a reduced short circuit current. This happens because, as the bandgap is raised, the minimum energy of photons that can generate carriers in the semiconductor increases. Hence, fewer photons can now be useful for current generation. As it turns out, however, solar cell modules can actually benefit from this effect, because when the current ($I_{SC}$) decreases, the resistive losses in the modules also decrease. In addition to these effects on $V_{OC}$ and $I_{SC}$, there are a few more advantages of having a high bandgap absorber layer, and these will be discussed in a later section dealing with CuGaSe$_2$.

One of the advantages of compound semiconductor thin film technologies is that different compounds can be alloyed together to form newer compounds, to achieve the desired material properties. The CuInSe$_2$ family includes a variety of such ternary semiconductor compounds that can be considered for alloying, some examples of which are tabulated on the next page (Table 3.1), along with their respective bandgaps values [Gabor, 1995].
Table 3.1. Various Ternary Absorber Materials with their Bandgaps [Gabor, 1995]

<table>
<thead>
<tr>
<th>Absorber Compound</th>
<th>Bandgap (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CuInSe$_2$</td>
<td>1.04</td>
</tr>
<tr>
<td>CuGaSe$_2$</td>
<td>1.70</td>
</tr>
<tr>
<td>CuAlSe$_2$</td>
<td>2.70</td>
</tr>
<tr>
<td>CuInS$_2$</td>
<td>1.55</td>
</tr>
<tr>
<td>AgInSe$_2$</td>
<td>1.24</td>
</tr>
<tr>
<td>CuInTe$_2$</td>
<td>0.95</td>
</tr>
</tbody>
</table>

Recent calculations show that, given the shape of the AM1.5 global solar power spectrum, the ideal bandgap for efficient solar energy conversion is around 1.14eV [Ward, 1993]. It will, therefore, be advantageous to alloy CuInSe$_2$ with higher bandgap materials to achieve a better match to the solar spectrum. One of the most promising ways to increase the bandgap of CuInSe$_2$ is to incorporate gallium (Ga). It can be seen, from the first two entries of the above list, that, if In is replaced by Ga, the bandgap of the absorber increases from 1.04 to about 1.70eV, a jump of 0.66eV! The specific advantages of the CuGaSe$_2$ material will be discussed later. An extremely important case, however, is a quaternary compound CuIn(Ga)Se$_2$, where only a part of the In in the basic CuInSe$_2$ is replaced by Ga, so that the resulting material becomes an alloy of CuInSe$_2$ and CuGaSe$_2$. The bandgap of this alloy material can be varied between the two extreme values mentioned above, and it can also be varied as a function of the depth within the absorber layer itself. This CuIn(Ga)Se$_2$ material has been extensively explored in the recent past, and is discussed next.
3.3.3. CuIn(Ga)Se$_2$

CuIn(Ga)Se$_2$ solar cells, prepared by incorporation of a controlled amount of gallium, have recently reached 18.8% efficiency, which is the highest efficiency ever reported for a thin film solar cell [Contreras, 1999].

As mentioned in the last section, when In in CuInSe$_2$ is replaced by Ga, the bandgap tends to increase. Evidently, this is an effect of the smaller size of the Ga atom (when compared with In), and the various formation energies involved. Albin carried out optical absorption measurements, and determined the bandgaps of CuInSe$_2$-CuGaSe$_2$ alloys over the full range of compositions [Albin, 1990]. According to him, for CuIn$_{1-x}$Ga$_x$Se$_2$, the bandgap varies according to

$$E_g = 1.011 + 0.664x - 0.249(1-x)$$

(Eq. 3.1)

and, for films with slight Cu deficiencies, the relation becomes linear, with

$$E_g = 1.0032 + 0.71369(1-x)$$

(Eq. 3.2)

Both these functions are shown in the following figure.

![Figure 3.3. The CuInSe$_2$ Structure [Albin, 1990]](image-url)
With the addition of Ga, and the corresponding change in the bandgap, some of the material properties also change. These include structural properties like lattice constants, film morphology and adhesion, and chemical changes such as defect levels, affinities and carrier concentrations. Therefore, the In to Ga ratio must be optimized to achieve the appropriate set of film properties, and thereby obtain highest possible performance of the solar cell devices. At present, the best CuIn$_{1-x}$(Ga$_x$)Se$_2$ solar cells are made with $x \leq 0.3$.

Wei, et al. have listed the effects of Ga addition to CuInSe$_2$, which are the following [Wei, 1998].

First, Ga incorporation increases the bandgap, according to [Albin, 1991]:

$$E_g(x) = (1-x)E_g(CuInSe_2) + xE_g(CuGaSe_2) - bx(1-x)$$  \hspace{1cm} (Eq. 3.3)

where $b$ is the (measured) bowing coefficient that depends on growth. The theoretical value of $b$ has been calculated to be 0.21, in good agreement with the most reproducible experimental values of 0.15 to 0.24 eV. Second, the hole concentration in the stoichiometric 1:1:2 compound increases significantly. In addition, the stability domain of the 1:1:2 compound in the phase diagram increases, i.e., the chalcopyrite phase becomes more stable, while the 1:3:5 ordered defect compounds (ODC) now have a narrower domain of existence in the phase diagram. As $x_{Ga}$ increases, the cell efficiency initially increases. However, when $x > 0.3$, the efficiency drops off. The 1:1:2 phase can no longer be made n-type. It has been previously suggested that the reason for this performance deterioration is related to strain, which comes from the lattice mismatch between the 1:1:2 and the 1:3:5 phases at the interface, as $x_{Ga}$ goes over 0.3, causing structural defects. However, the calculation of Wei, et al. shows that the change of the
lattice mismatch due to Ga addition is very small, and hence is unlikely to be the main reason for device deterioration.

As mentioned once before, the bandgap in the p-type CuIn(Ga)Se$_2$ absorber layer can actually be engineered so that it changes rather gradually, from the metallurgical junction towards the inside of the absorber. This is made possible by changing the Ga concentration (that is, the Ga/(Ga + In) ratio) with the depth of the film. An illuminating account of how this can be achieved has been given by Gabor [Gabor, 1995]. The effect can be briefly explained as follows.

![Figure 3.4. Band Bending with (a) No Grading, and (b) Grading](image)

The above figure depicts two different structures, one with a single bandgap throughout the absorber layer, and the other with a graded bandgap (the bandgap increasing towards the back). As will be discussed later, in CuIn(Ga)Se$_2$, the bandgap increase, arising because of Ga incorporation, seems to be accommodated by the conduction band edge moving upwards. If a single bandgap exists throughout the thickness of the absorber layer, then the band bending is confined to the front portion of the layer, in the region where the depletion region penetrates. (This, of course, depends
on the doping level in the film.) Hence, there is no electric field outside this region, towards the back of the device. The minority carriers (electrons in the conduction band, in the case of CuIn(Ga)Se$_2$), that are generated outside the depletion region, therefore, must rely on the diffusion mechanism to reach the junction. If, however, the minority carrier diffusion length is small, compared to the depth of the absorber layer beyond the depletion region, then carriers generated far away from the depletion region (i.e., towards the back of the layer) have only a small probability of being collected, and of contributing to the photocurrent. On the other hand is the other structure, where a bandgap grading, and the resulting conduction band edge bending, exists. In this case, the quasielectric field helps the electrons move towards the front of the device, thereby increasing the probability of their collection.

The above example demonstrates that it is important to gain a precise control over the composition throughout the depth of the film. By having such a control, the intended grading profile can be carefully accomplished. On the other hand, if no grading is intended, any grading can be avoided, using carefully controlled compositions. Any unintentional grading in the opposite direction (bandgap decreasing towards the back) may seriously hurt the collection efficiency of the device.

Fortunately, the latter effect, of the existence of an opposite grading, is easily avoided in CuIn(Ga)Se$_2$ processing. It turns out that Ga in the films has a strong tendency to move towards the back of the device, with In staying at the front. Such an effect means that it is easy to get the bandgap to increase towards the back. However, this creates another challenge for the processing engineers. Because the Ga will always try to go deeper, it becomes more difficult to create a thin higher-bandgap layer at the
front, when one intends to utilize the increased bandgap offered by CuGaSe$_2$ to increase the $V_{OC}$ of the solar cell.

3.4. CuGaSe$_2$ Solar Cells

3.4.1. Advantages of a High Bandgap

Before we go on to the specifics of the CuGaSe$_2$ solar cell devices, it will be worthwhile to list the various advantages of having a higher bandgap for the absorber material (some of which have been mentioned before).

(i) The open circuit voltage, obtainable from a solar cell, is proportional to the bandgap of the absorber. Hence, as the bandgap increases, so does the $V_{OC}$. The current density, on the other hand, decreases with an increasing bandgap. However, this loss in the current density means lower ohmic losses in the solar cell modules, which is an important advantage.

(ii) With increased $V_{OC}$’s, fewer cells are needed to obtain the given voltage. Consequently, the number of interconnects within the module is reduced, thereby lowering the optical losses.

(iii) The relative loss of the open circuit voltage with increased temperature is significantly lower for wider bandgap materials [Nadenau, 1999].

(iv) High bandgap materials have the potential to be used in tandem solar cells.

(v) (Specific to devices based on CuInSe$_2$-type absorbers.) In the solar cells based on CuInSe$_2$, the bulk of the series resistance comes from the ZnO, which is the
common front contact/window material. To reduce this resistance, the doping in ZnO has to be made very high. However, this gives rise to another problem. At around 1.1 eV (approximately 1100 nm), the highly doped ZnO starts to show high free carrier absorption, thereby reducing the photocurrent in that wavelength range. If the bandgap of the absorber is increased significantly such that the photocurrent no longer depends on these high wavelengths, then the loss because of the free carrier absorption does not hurt the device any more. This is easily accomplished with CuGaSe$_2$, as the relevant absorption wavelengths are well below the above-mentioned range.

3.4.2. CuGaSe$_2$ Device Issues

3.4.2.1. High Bandgap and $V_{OC}$ Limitation

With a bandgap of 1.68 eV at room temperature, CuGaSe$_2$ is a good candidate for high voltage single cell devices, as well as for the top cell in tandem systems. Due to its high optical absorption coefficient, it is suitable for thin film applications.

The typical device structure (one which has shown most promise for high performance) for a solar cell device using a CuGaSe$_2$ absorber layer is: Glass/ Mo Back Contact/ p-CuGaSe$_2$/ n-CdS/ ZnO Front Contact, which is essentially the same as that for a CuInSe$_2$ device, with the CuInSe$_2$ absorber layer replaced by CuGaSe$_2$.

As mentioned previously, the higher bandgap of CuGaSe$_2$ means less current density. In the case of CuGaSe$_2$, only the photons below about 750 nm are absorbed
strongly, leading to fewer photo-generated carriers. In CuInSe₂, the corresponding wavelength is about 1200 nm. The unused range (difference between the two) of almost 450 nm usually translates into a loss of more than 20 mA/cm² for a typical laboratory device.

Equations (3.1) and (3.2), presented before, related the bandgap increase to the amount of Ga incorporated into CuInSe₂. In fact, a phenomenological relation can be given for the Vₜₜₜ’s in Ga-containing devices, which is [Nadenau, 1999]:

\[
V_{oc} = \left( \frac{E_g}{q} \right) - 500 \text{mV} \quad \text{(Eq. 3.4)}
\]

Here \(E_g\) is the bandgap, and \(q\) is the elementary charge. According to this relation, CuGaSe₂, with its bandgap of 1.68 eV, should exhibit voltages as high as 1.2 V. Until 1997, even after a couple of decades of CuGaSe₂ research, the best Vₜₜₜ’s were still limited to about 750 mV. Later that year, Nadenau et al. used a new processing approach, and succeeded in preparing CuGaSe₂ devices with a Vₜₜₜ of 870 mV and a conversion efficiency of 9.3% [Nadenau, 1997]. This performance has been the best so far, for thin film polycrystalline CuGaSe₂. The cells in this case were processed using a newly optimized deposition temperature for the CdS buffer layer. For comparison, the best efficiency for a single-crystal CuGaSe₂ solar cell device is 9.7% [Saad, 1996].

As already mentioned, Vₜₜₜ’s of 870 mV have been achieved for CuGaSe₂ solar cells. However, the theoretical and phenomenological models seem to indicate that there is another about 300 mV that should be obtainable for this material. A few studies have been carried out to investigate the limiting mechanisms that seem to have held the Vₜₜₜ’s hostage, and to understand the transport mechanisms that are involved. An extensive review of these studies will now be presented. But before that, let’s revisit a couple of
important aspects of the CuInSe$_2$/CuGaSe$_2$ absorber materials, so that the survey of the results can be easily understood.

Firstly, there is the change in the band diagram, and hence in the band bending, because of Ga incorporation. When a band gap increases, the change could be because of the valence band edge $E_V$ moving downwards, or the conduction band edge $E_C$ moving upwards, or a little of both. The evidence seems to suggest that the bandgap change in the case of CuGaSe$_2$ comes from the change in the electron affinity, and hence from the conduction band moving upwards. The second important aspect relates to the various point defects, the important ones being the vacancies, antisite defects and interstitials. It should be remembered that these are native defects, and hence are not very easily controlled by changes in the processing conditions. Nevertheless, factors such as the formation energies of the defects have tremendous impact on the doping levels and other parameters that govern the performance of the devices. Another aspect that is closely related with the defects is the doping inversion (the ODC’s) that is present in the CuInSe$_2$ absorber. Such a layer could significantly alter the device performance. For example, if the inverted layer is thick enough, it essentially makes the junction a buried homojunction, rather than a true heterojunction. Because the electrical junction is now well below the metallurgical CuInSe$_2$/CdS junction, it is relatively protected from any possible structural defects or strains that can form at the metallurgical interface between the two semiconductors. Whether or not such an inverted layer can be formed (and if it is formed, how much its thickness and degree of inversion is), therefore, will play a significant role in determining the junction characteristics.
3.4.2.2. Band Discontinuities and Surface Inversion

Wei, et al. used a first-principles band structure method to theoretically study the effects of Ga addition on the electronic and structural properties of CuInSe$_2$ [Wei, 1998]. Some of their findings are summarized below.

The band offset $\Delta E_V$ between the valence band maxima of CuGaSe$_2$ and CuInSe$_2$ was calculated to be only 0.04 eV, when CuGaSe$_2$ and CuInSe$_2$ each have their own equilibrium lattice constants. Therefore, it could be concluded that the conduction band minimum ($E_C$) of CuGaSe$_2$ was about 0.6 eV higher than that of CuInSe$_2$. (The relation $\Delta E_C = \Delta E_G - \Delta E_V$ has been used.) This is shown in the Figure 3.5, where the band diagrams of three ternary chalcopyrite compounds, CuInSe$_2$, CuGaSe$_2$ and CuAlSe$_2$, are compared.

The above calculation also suggested that p-type doping in CuInSe$_2$ and CuGaSe$_2$ should be similar, while n-type doping should be more difficult in CuGaSe$_2$ than in CuInSe$_2$.

Figure 3.6 presents the calculated band offsets, in eV, between CdS, CuInSe$_2$ and CuIn$_x$Se$_5$ [Zhang, 1998]. The offset between CdS and CuGaSe$_2$ can be easily visualized, with the CB of the absorber moving upwards by about 0.6 eV.
The calculated defect formation energies $\Delta E$ of single acceptor defects ($V_{Cu}$, $V_{Ga}$, and $Cu_{Ga}$) in $CuGaSe_2$ were found to be similar to their counterparts in $CuInSe_2$, meaning that the acceptor densities in the two compounds are similar. However, the formation
energies of single donor defects ($\text{Ga}_{\text{Cu}}^0$, $\text{Cu}_i^0$) in CuGaSe$_2$ were larger in CuGaSe$_2$, when compared to those in CuInSe$_2$, so that the donor density in CuGaSe$_2$ could be lower than that in CuInSe$_2$, under similar growth conditions.

A comparison of the defect transition energy levels showed that the acceptor levels in CuGaSe$_2$ were similar to, or slightly shallower than, those in CuInSe$_2$, suggesting the presence of slightly more holes in CuGaSe$_2$. On the other hand, the $\text{Ga}_{\text{Cu}}$ antisite donor levels in CuGaSe$_2$ were much deeper than the $\text{In}_{\text{Cu}}$ donor levels in CuInSe$_2$. This meant that, as far as the contribution of III-on-I antisite defects to $n$-typeness was concerned, CuGaSe$_2$ would be less $n$-type than CuInSe$_2$.

3.4.2.3. CuGaSe$_2$ Transport Mechanisms

In a recent paper, Nadenau, et al. presented a systematic study of the electronic transport mechanisms of CuGaSe$_2$-based solar cells [Nadenau, 2000]. They tried to relate these mechanisms to the stoichiometry deviations, the substrates, and the buffer layers. Their findings are discussed below in detail. The evaluation models used by the authors are briefly mentioned, followed by their experimental results.

First, the authors recognize that in the case of low Ga content (Ga/(Ga + In) below 0.3), the Fermi level at the surface of the absorber is closer to the conduction band, and hence this surface is inverted. They hence argue that this type-inversion at the interface decreases the number of available holes at the interface, thereby diminishing interface recombination, so that the recombination in the space-charge region (SCR) becomes the dominant loss mechanism. With the help of admittance spectroscopy, the authors show
that this type-inversion is not exhibited in CuGaSe$_2$/CdS/ZnO devices. The following heterostructure band diagram (reproduced from the publication), under an applied bias voltage, depicts the possible recombination paths in this solar cell structure.

![Band Diagram](image)

**Figure 3.7. Band Diagram** (a) at Equilibrium, (b) at an Applied Bias

Second, the authors argue that the space charge in these solar cells extends into the CdS buffer as well as the ZnO window layer, and a large density of electrons is
available in the buffer layer due to the negative band offset between the absorber and the buffer material.

The authors then go on to treat the *Tunneling Enhanced Interface Recombination* as well as the *Tunneling Enhanced Bulk Recombination*. These equations are then combined to formally describe the forward current density $J$ as

$$J = J_0 \exp \left( \frac{qV}{AKT} \right) = J_{00} \exp \left( -\frac{E_a}{AKT} \right) \exp \left( \frac{qV}{AKT} \right)$$  \hspace{1cm} (Eq. 3.5)

with $J_0$ as the saturation current density. The open circuit voltage can then be given as

$$V_{OC} \approx \frac{AKT}{q} \ln \left( \frac{J_{SC}}{J_0} \right) = \frac{E_a}{q} - \frac{AKT}{q} \ln \frac{J_{00}}{J_{SC}}$$  \hspace{1cm} (Eq. 3.6)

If $A$, $J_{SC}$ and $J_{00}$ are independent of temperature, a plot of $V_{OC}$ vs $T$ should yield a straight line and the extrapolation of this line to $T = 0^\circ K$ should give the activation energy $E_a$. This activation energy corresponds to the flatband barrier $\Phi_{bf}$ ($\Phi_{bp}$ if the barrier height is not field-dependent) in the case of *interface recombination*, and to the bandgap energy $E_g$ in the case of *bulk recombination*.

Also, when tunneling is important, the ideality factor becomes temperature-dependent, and hence the authors use the $J_0$ equation to get

$$A \ln \left( J_0 \right) = -\frac{E_a}{kT} + A \ln \left( J_{00} \right)$$  \hspace{1cm} (Eq. 3.7)

Here, the plot of $A \ln \left( J_0 \right)$ vs. inverse temperature $1/T$ should yield a straight line with a slope corresponding to the activation energy $E_a$. This activation energy is the flatband barrier $\Phi_{bf}$ and bandgap energy $E_g$ in the case of interface recombination and bulk recombination, respectively.
The authors examined two sets of CuGaSe$_2$ samples: Cu-rich and Cu-poor (i.e., Ga-rich). Each of these categories had one Na-containing and one Na-free sample. The temperature-dependence of the $V_{OC}$ was measured, and the activation energy $E_a$ for the dominant recombination process was found from the extrapolation of the plot on the voltage axis. For the Cu-rich devices, an $E_a \sim 1.25$ eV was identified as the flat-band barrier, assuming *interface* recombination (alternatively, this $E_a$ could also be identified with the presence of Cu$_7$Se$_4$ precipitates). In contrast, the Na-containing Ga-rich devices had an $E_a \sim 1.6$ eV, thereby indicating that the recombination mechanism which limited $V_{OC}$ occurred in the *volume* (bulk) of the absorber material.

The temperature dependence (125-350°K) of the inverse (diode) ideality factors (1/A) was used for the quantitative analysis of the I-V data of the different CuGaSe$_2$ devices. The Cu-rich, Na-containing device showed the largest ideality factors over the whole temperature range, with the product $AT$ being independent of temperature, suggesting that tunneling was the dominant recombination mechanism. These devices also exhibited higher values of saturation current densities. On the other hand, the Ga-rich samples showed reduced values of saturation current densities near room temperature, and also lower values of diode ideality factor. These were fitted to obtain lower values of tunneling energy and of charge density, than those of the Cu-rich samples.

The authors then monitored the change in the capacitance and $V_{OC}$, during the light soaking of the samples using red light of wavelength > 630nm. For both, Cu-rich/Na-free as well as Ga-rich/Na-containing, samples, the capacitance rose during illumination, indicating increased space charge density (and a corresponding decrease in
the SCR width). The $V_{OC}$, however, behaved differently for the two devices. The Cu-rich device showed a decrease, whereas the Ga-rich device exhibited an increase in the $V_{OC}$. It was then concluded that *tunneling-enhanced interface recombination* process dominated the *Cu-rich* devices, whereas the dominant process in the *Ga-rich* devices was *recombination in the SCR without significant contribution from tunneling*.

It was also proposed by the authors that the reduction of space charge density, in the case of the Ga-rich devices optimized with the improved CdS buffer deposition process, was the result of Cd diffusion. The formation of Cd$_{Cu}^+$, according to the authors, might have compensated for the high concentration of negatively charged Cu-vacancies ($V_{Cu}^-$) within the defective surface layer. This issue of the effect of the buffer layer deposition will be discussed in more detail in the next section.

In the part II of the above-mentioned study, Jasenek, et al. studied the electronic properties of the Cu-rich and Ga-rich CuGaSe$_2$ devices using admittance spectroscopy, DLTS, and C-V measurements [Jasenek, 2000]. Using a recently determined band offset value $\Delta E_V$ of 0.9 eV at the CuGaSe$_2$/CdS interface, the energetic difference $E_F-E_V$ was calculated to be 0.8 eV, as shown in the following figure.
In the above model, the CdS buffer layer is assumed to be completely depleted. It can also be easily seen that there is no type-inversion at the surface of the CuGaSe$_2$ absorber layer.

For the Cu-rich samples, the defect spectra resulted from two different emissions, A1 and A2, which were correlated to two different acceptor-like bulk traps, with activation energies of 240 meV and 375 meV, respectively. Trap A1, with a concentration of $4 \times 10^{17}$ cm$^{-3}$ eV$^{-1}$ yielded the dominant emission, whereas trap A2 concentration was lower by a factor of 5. Air-annealing was found to reduce the density of A1 to some extent, whereas the density of A2 was drastically reduced, thereby implying that annealing affected deeper traps more. It was also suggested that the defect A2 might reflect a Ga vacancy $V_{Ga}$, and A1 might be correlated to either another transition of $V_{Ga}$, or a Cu$_{Ga}$ antisite defect.
The Ga-rich sample, on the other hand, exhibited a tail-like energy distribution of acceptor defects, with the maximum lying at about 250 meV. This defect, it was concluded, provided the dominant recombination path in high-efficiency CuGaSe$_2$ solar cells based on Ga-rich absorbers. Another important result was that the performance limitation of these CuGaSe$_2$ devices mainly originated from the low electronic quality of the absorber, and not that of the film surface.

### 3.4.2.4. Effect of Buffer Deposition

It must be remembered that, in the substrate type CuGaSe$_2$ solar cell preparation, the CdS buffer/heterojunction partner is deposited after the absorber layer. Hence, the substrate sees the atmosphere while it is being transferred from the absorber deposition vacuum chamber to the CdS bath. It may take several minutes before the sample is actually dipped in the CdS bath. A strong sensitivity of CuGaSe$_2$-based solar cells to air exposure time of the absorber surface after growth before deposition of the buffer layer has been reported leading to a drastic degradation of the device performance [Nadenau, 1997]. Such a strong dependence of the performance on the processing variables relating to the surface of the absorber suggests that the junction formation and/or the junction transport mechanisms in the case of CuGaSe$_2$ may correspond to those of a true heterojunction, rather than to a buried homojunction.

Even in the case of a CuIn(Ga)Se$_2$/CdS interface, with a buried electronic junction, intermixing has been observed at the interface. For example, Heske, et al. carried out a combination of x-ray emission spectroscopy and x-ray photoelectron
spectroscopy using high brightness synchrotron radiation of such a buried interface [Heske, 1999]. Samples were prepared by rapid thermal processing of Cu, In, Ga and Se layers, followed by chemical deposition of CdS. Intermixing processes involving S, Se and In were identified in the analysis.

As mentioned earlier, the best performance for a CuGaSe$_2$ solar cell has been obtained by using a newly optimized buffer layer [Nadenau, 1997]. The older buffer deposition process had used a temperature of $60^\circ$C. The chemistry of the CdS bath was changed (the concentration of NH$_3$ in the bath was increased) so that the deposition temperature in the new process rose to $80^\circ$C. A CuGaSe$_2$ device that used a Ga-rich absorber layer had the best performance. There are several possible reasons for this performance improvement resulting from the new CdS process, and these are outlined below.

Nadenau, et al. compared two Cu-rich samples treated with KCN after the deposition [Nadenau, 1999]. The KCN treatment was carried out to remove the unwanted Cu-Se species present at/near the absorber surface. One of the samples went through a $60^\circ$C CdS process, while the other went through an $80^\circ$C process. The performance of the $80^\circ$C sample was actually diminished, compared to the $60^\circ$C sample (a trend opposite to that seen for CuGaSe$_2$ made using Ga-rich absorber film). EDX linescans across the interfaces of these samples showed that the interaction between Cu and the buffer layer was much stronger for the $80^\circ$C CdS sample. From the analysis of the microstructures of these Cu-rich and Ga-rich samples, it could be concluded that:
(i) For all devices based on Cu-rich (KCN-treated) absorber layers (both, 60° C, as well as 80° C CdS), and also for the device based on Ga-rich layer with 60° C CdS, the recombination at the interface was dominant.

(ii) For Ga-rich absorber devices with 80° C CdS, recombination in the space charge layer was dominant. The interfacial region for this sample was found to be spatially enlarged, leading to a lower density of interfacial states. Moreover, the lattice mismatch between CuGaSe₂ and CdS was reduced due to the dominant cubic phase of CdS for the 80° C recipe. Using XPS measurement results, it was also proposed that sulfur was incorporated in the place of selenium at the top of the absorber layer, thereby decreasing the valence band energy there. This created a front surface field close to the interface, pushing the holes back into the absorber layer, thereby reducing the number of carriers contributing to the interfacial recombination.

In another study (that has been previously cited) Nadenau, et al. have compared the diode ideality factors for two Ga-rich, Na-containing samples with different CdS deposition temperatures [Nadenau, 2000]. The following figure, reproduced from the publication, shows the variation of the inverse ideality factors with the absolute temperature.
Figure 3.9. Variation of the Inverse Diode Factor with Temperature

The $80^0\text{C}$ CdS device exhibited the lowest values of $A$, which were below 2 at room temperature. The calculated tunneling energy, deduced using the tunneling theory (briefly outlined before), for the $80^0\text{C}$ device (23 meV) was much lower than that for the $60^0\text{C}$ device (42 meV). It was hence concluded that the reduction of tunneling losses by the higher temperature CdS process was crucial for the better performance of these devices. The model that was proposed to explain the beneficial effect of the increased CdS bath temperature was the following. It had been suggested, from earlier studies, that the Cu-poor surface layer of high-efficiency CuIn(Ga)Se$_2$ films was a result of Cu removal from the surface via the creation of Cu vacancies $V_{\text{Cu}}^{-}$ and the migration of Cu interstitials into the bulk of the absorber material [Klein, 1999]. This migration led to a high concentration of negatively charged $V_{\text{Cu}}^{-}$ within a defective surface layer [Niemegeers, 1998]. Such a high charge density would enhance tunneling. However, if Cd ions could diffuse into the grains of the absorber, the formation of Cd$_{\text{Cu}}^{+}$ could
compensate a part of this charge, thereby reducing the tunneling. The observed decrease of the tunneling energy for the higher temperature CdS deposition process was hence consistent with a stronger Cd diffusion into the absorber.

The above model agrees well with another study, performed by Nakada, et al., for the case of high efficiency CuIn(Ga)Se$_2$ solar cells [Nakada, 1999]. They investigated the diffusion behavior at the CuIn(Ga)Se$_2$/CdS interface, using EDS. The analysis revealed that Cd was present in the CuIn(Ga)Se$_2$ layer approximately 100 Å from the interface boundary, thereby giving a direct evidence of Cd diffusion. Also, Cu concentration was found to be decreased near the surface of the absorber film, suggesting substitution of Cd for Cu atoms.

3.4.2.5. Effect of Post-Deposition Treatments

Several groups have reported an enhancement of the performance of CuInSe$_2$ or CuIn(Ga)Se$_2$ devices after a post-deposition air-annealing treatment. It has been proposed that oxygen passivates surface dangling bonds related to Se deficiencies. This, in turn, reduces grain-boundary recombination, enhances the net p-type doping of the absorber, and facilitates inter-grain transport [Cahen, 1991]. However, at times, contradictory results are reported for different fabrication processes used. Rau, et al. studied air-annealing effects on CuIn(Ga)Se$_2$ films with the help of photoelectron spectroscopy and admittance spectroscopy [Rau, 1999]. UV photoelectron spectroscopy revealed type-inversion at the surface of as-made films, which disappeared after exposure of several minutes to air, due to the passivation of surface Se deficiencies. XPS revealed
that air-annealing at 200°C led to a decreased Cu concentration at the film surface. Admittance spectroscopy of completed CuIn(Ga)Se$_2$/CdS/ZnO devices showed that the absorber surface type-inversion was restored by the chemical bath used for CdS deposition. Air-annealing of these finished devices at 200°C reduced the type-inversion again, due to defect passivation. Moreover, the study also showed that oxygenation led to a charge redistribution and to a significant compensation of the effective acceptor density in the bulk of the absorber, suggesting the release of Cu from the surface and its redistribution in the bulk.

For Ga-rich CuGaSe$_2$ devices, Jasenek, et al. found improved performance after an air-anneal. A study of the change in the diode ideality factors and a numerical fit to the tunneling model indicated that the tunneling energy reduced significantly after the anneal. However, an Arrhenius plot of $[A \ln(J_0)]$ Vs. $1/T$ showed that the activation energy remained nearly constant, indicating that recombination in the SCR was still the dominant recombination mechanism.

**3.4.2.6. Other CuGaSe$_2$ Issues**

Kampschulte, et al. carried out measurements of some important parameters of the CuGaSe$_2$ material, such as mobility and resistivity [Kampschulte]. They studied CuGaSe$_2$ epitaxial layers that were grown on GaAs(001) substrates by low pressure metalorganic vapor phase epitaxy (MOVPE), exclusively with metalorganic precursors. XRD measurements revealed a predominantly c[001]-oriented growth. All these CuGaSe$_2$ layers showed p-type conductivity with net carrier concentrations of the order
of $10^{17}/\text{cm}^3$ and Hall mobilities of approximately $30 \text{ cm}^2/\text{V-s}$. Also, the resistivity of 260 nm thick layers was found to be in the range of $0.5-1 \Omega \cdot \text{cm}$. MOVPE was utilized with the future purpose of using the same reactor sequentially to grow the heterojunction partner $n$-ZnSe, so that the sample would not be exposed in between.
4.1. The Device Structure

The fabrication of the CuIn(Ga)Se$_2$ or CuGaSe$_2$ solar cells involves a sequential deposition of the various thin films that serve specific purposes, such as the absorber material, the buffer, and the front and the back contacts. The overall structure can be written as: Glass substrate/ Molybdenum (Back Contact)/ CuIn(Ga)Se$_2$ or CuGaSe$_2$ (Absorber material)/ CdS (n-type Buffer)/ ZnO (Front contact), deposited in this sequence. The following figure depicts this structure.

Figure 4.1. Structure of Our Typical Solar Cell Device
4.2. Fabrication of CuGaSe$_2$ Solar Cells

4.2.1. A Manufacturing-Friendly Process

Our laboratory has been developing a manufacturing-friendly process for CuIn(Ga)Se$_2$ and CuGaSe$_2$ solar cell preparation for the past few years. The manufacturing-friendliness of the process has two aspects, as discussed below.

Firstly, our fabrication involves a two-step process for the preparation of the absorber layer. The first step is the deposition of the metal precursors (deposited sequentially from individual metal sources), and the second step is the high temperature selenization. As mentioned previously, such a process has distinct advantages compared with the more common co-evaporation process used by some other laboratories. The co-evaporation technique (obviously) requires a very high degree of control, because a number of elements are being evaporated from different sources simultaneously. This is especially important in the case of ternary or quaternary compounds such as those dealt with in this research. Therefore, the size of the substrate can be severely limited when co-evaporation is being used, for larger substrate sizes usually mean more non-uniformity of the film composition. The two-step process, on the other hand, is relatively easily scaleable to commercial production, and hence can be termed as manufacturing-friendly.

The second aspect of manufacturing-friendliness comes from a rather undesirable, however, unavoidable, situation. Our laboratory, by the virtue of being a part of a University, faces several restrictions. First of all, there’s always the financial funding problem. This often means that there are limitations as regards the quality of vacuum
systems, that of the maintenance, and such. There are several graduate students walking around, sometimes leaving the doors to the laboratory wide open, and bringing the outside dust and other impurities in. It’s not exactly a clean-room situation. There’s limited space to move around, and the samples have to be carried by hand from one room to another between depositions. A process that is developed in our laboratory, therefore, would automatically be a robust process, and any further improvements in terms of deposition systems or the processing environment, such as those that would ensue in a highly maintained commercial method, would likely lead to an improvement of the device performance.

The processing of the various thin films will now be described, along with the important characteristics of each of the material layers. (The absorber material, which is the most important material of interest, will be discussed last.)

It should be kept in mind that one of the main aims of solar cell development is to arrive at a process that offers a low-cost electricity-generation method. Hence, simple and cost-effective deposition techniques, as well as inexpensive materials, have been preferred over their costly alternatives.

4.2.2. The Substrate

The choice for the substrate material is Soda-Lime Glass. It is an inexpensive substrate material, and offers good resistance to corrosion. It is also easily available at local hardware stores. There are other advantages associated with the use of glass as the substrate, such as, the substrate can be used as a packaging material. This becomes even
more important when the solar cells are superstrate-type, where the light is shone through the glass to reach the absorber. Another benefit of using soda-lime glass is the diffusion of sodium (Na) from the glass to the deposited layers. In CuInSe\textsubscript{2}-type cells, the $V_{OC}$’s have been shown to increase because of this Na reaching the absorber films.

There are a few disadvantages that are associated with the use of soda-lime glass. Firstly, the operating temperatures have to be limited to about 600\textdegree C, otherwise the glass is prone to warping, or even breakage, because of the stress. Secondly, the glass pieces purchased from local stores sometimes have scratches and/or spots on them, which can degrade the structure, and hence the performance, of the films deposited on them. It, therefore, becomes crucially important that the glasses are thoroughly cleaned before they are used.

The cleaning procedure involves a soap/DI water soak step, followed by a soap-scrub and DI water rinse. The glass pieces then go through an ultrasonic clean in a chemical (trichlorotrifuoroethane) that removes the organics from the glass. This is again followed by a DI water rinse. Lastly, the glass is blow-dried with high-purity nitrogen.

4.2.3. The Back Contact

Molybdenum (Mo) is a refractory metal that has been widely used as a contact material for CuInSe\textsubscript{2}-type solar cells. It forms a good ohmic contact, and has a high resistance to selenium corrosion.

A 1 \textmu m thick molybdenum layer is deposited using DC magnetron sputtering. Before this deposition, the glass is often heated in vacuum, to get rid of the moisture
present. It has been shown that the sputtering pressure is crucially important to the quality of the films. If deposited at higher pressures, the films exhibit a rough surface morphology and poor resistivity, but they adhere well to the underlying glass substrate. On the other hand, films deposited at lower sputtering pressures have improved resistivity and smoother surfaces, but they suffer from adhesion problems due to compressive stress. To circumvent this problem, Scofield, et al. used a bi-layer of Mo, where the two layers were deposited at two different pressures (Scofield, 1995). Such a bi-layer has been used for our molybdenum deposition. A thin first layer (of about a 1000 A$^0$), is deposited at a higher pressure of about 5 mTorr, to get the improved adhesion, followed by a low-pressure (~1.5 mTorr) layer that gives excellent conductivity (typical numbers for the resistivity are in the low $10^{-5}$ Ω-cm range).

4.2.4. The Heterojunction Partner/ Buffer

Cadmium Sulfide (CdS) has been used extensively as the n-type semiconductor material to form the p-n junction with the p-type CuGaSe$_2$ absorber material. CdS has a direct bandgap of 2.4 eV, and has an absorption edge at around 510 nm. This means that some of the light in the blue region of the visible solar spectrum (that below 510 nm) is absorbed in the CdS layer. These absorbed photons can generate carriers, and such carriers can also contribute to the total photogenerated current. All the photons that have energy lower than 2.4 eV (i.e. wavelength higher than 510 nm) are transmitted through the CdS layer into the absorber layer.
The CdS film is deposited by the Chemical Bath Deposition (CBD) technique. CBD is a non-vacuum process, which turns out to be the best method for the CdS deposition so far. Other techniques, such as Close-Space-Sublimation and Sputtering, have been experimented with. However, these methods have produced CdS layers that severely limit the performance of the solar cells. This has been attributed to the possible cleaning and/or passivation of absorber surface by the chemicals involved in the CdS bath.

The CdS layer, evidently, plays an additional role. The CdS deposition comes after the absorber layer, and before the ZnO front contact. ZnO is deposited by RF sputtering, which, if done directly after the absorber, could severely damage the surface of the absorber layer. The CdS essentially protects the absorber surface from this damage. Because of this, the CdS has often been referred to as the buffer layer in the literature.

The chemistry of the deposition involves Cadmium Acetate (a source for the Cadmium), Thiourea (a source for Sulfur), and Ammonium Hydroxide (which acts as a complexing agent, controlling the rate of the reaction).

4.2.5. The Front Contact

A good front contact needs to satisfy two requirements. It has to be highly conductive, so that the current generated by the photons can easily be conducted into the external circuit. The sheet resistance of this layer needs to be as low as possible, because often the external metal grid is a set of thin metal fingers, separated by a significant
distance between them. The current, hence, has to also flow in a direction perpendicular to the direction of incident light. Secondly, the front contact material has to be as transparent to the incident photons as possible, so that they go through the layer unabsorbed, to reach the absorber layer. Zinc Oxide (ZnO) is used as the front contact for our solar cells. ZnO transmits about 90% of the incident light between 400 and 1000 nm. Transmission drops off at higher wavelengths, due to the free carrier absorption, which increases with increased doping. Therefore, a compromise has to be made in terms of achieving a low resistivity value and low free carrier absorption. Resistivity numbers of high $10^{-4}$ $\Omega$-cm are routinely achieved in our process.

After the CdS layer deposition, the sample is transferred to an RF sputtering system. An undoped ZnO layer of about 500 $\text{Å}$ is first deposited. This is then followed by a thicker (about 4500 $\text{Å}$) ZnO layer, which uses a ZnO target, along with several Aluminum pieces, to provide aluminum doping.

During the ZnO deposition, a mask is used to divide the 2”X 2” substrate into 25 individual circular device dots, each approximately of area 0.1 cm$^2$. This makes it easier to obtain good, working devices, without significant shunts. It also allows the performance variation between the individual devices to be correlated to the locations of the dots with respect to the deposition sources (this will be more clearly seen in a figure in the next section).
4.3. The Absorber

The absorber deposition system contains a substrate-holder, to hold the 2” X 2” substrate in place, and a heater system to heat the substrate. The evaporation sources for Cu, In, Ga and Se are located on four different sides, with respect to the substrate. This is depicted in the following figure.

![Figure 4.2. Arrangement of the Substrate and the Sources](image)

The above figure also shows four of the 25 circular device dots on one substrate (brought about with the help of a mask, during the ZnO deposition), along with the number system that is used to differentiate the individual devices.
As mentioned earlier, a sequential deposition process is more suitable than a co-deposition process, from the point of view of large-area commercial production of solar cell modules. Our process for the deposition of the absorber layer is a two-stage sequential process, these stages being:

(i) Precursor deposition: A low-temperature sequential deposition of Cu and Ga metals, either with or without a Se flux. (Cu, In and Ga in the case of CuIn(Ga)Se$_2$.)

(ii) Selenization: A relatively high-temperature step where the precursor film is annealed in a high flux of Se vapor.

It should be noted that, although the major part of this research project dealt with the development of a process for CuGaSe$_2$ absorber deposition, it did start out with optimization of our (regular) CuIn(Ga)Se$_2$ absorber process.

In the course of this research, various parameters for the absorber deposition were changed from time to time. Most of these films, however, could be divided into two major categories, depending on the sequence of the metal (Cu, Ga) depositions and the selenization temperature profiles. These two recipes are referred to as Type I and Type II CuGaSe$_2$, respectively, and are described next.

4.3.1. Type I Versus Type II

The first recipe used for CuGaSe$_2$ deposition, called Type I, was a natural extension of one of our CuIn(Ga)Se$_2$ deposition recipes, and involved the following sequence of depositions.
Type I CuGaSe$_2$:

(i) Precursor Deposition (275$^0$C):

   a. Initial Ga, 100 A$^0$,
   b. Ga and Se co-evaporation,
   c. Cu.

(ii) Selenization (Se evaporation, a flux of $\sim$ 28 A$^0$/s about 28 minutes total):

   a. Ramp up from 275 to 450 $^0$C,
   b. 7 minutes at 450 $^0$C,
   c. Ramp up from 450 to 550 $^0$C,
   d. 7 minutes at 550 $^0$C (30-40 A$^0$ Top Cu optional),
   e. Ramp down from 550 to 425 $^0$C.
   f. Cool-down to room temperature, in vacuum.

This sequence is summarized in the following figure.

![Figure 4.3. Time-Temperature Profile for Type I CuGaSe$_2$](image-url)
The Type II CuGaSe$_2$ also started with the same precursor deposition sequence 
(Ga/Ga-Se/Cu). However, about $4/5^{th}$ of the Ga needed for the absorber formation was deposited before the Cu. After the Cu deposition was over, the temperature was gradually increased all the way to 550 °C (eliminating the 450 °C step), along with a low Se flux (of about 12 A$^0$/s). The sample stayed at 550 °C for about 10 minutes, after which the remainder (about $4/5^{th}$ of the total amount) of the Ga was deposited, along with Se. This was then followed by 28 minutes of selenization in a high Se flux. The entire sequence can be divided into three parts as follows:

*Type 2 CuGaSe$_2$:*

(i) Precursor Deposition I (275 °C):
   a. Initial Ga, 100 A$^0$,
   b. Approx. $4/5^{th}$ Ga and Se co-evaporation,
   c. Cu.

(ii) Precursor Deposition II
   a. Ramp up from 275 to 550 °C (low Se flux),
   b. 10 minutes at 550 °C (low Se flux),
   c. Remaining Ga (low Se flux).

(iii) Selenization (Se evaporation, about 28 minutes total):
   a. 22 minutes at 550 °C,
   b. Ramp down from 550 to 425 °C.
   c. Cool down in vacuum.

This sequence of events is depicted in the following figure.
4.4. Characterization of CuGaSe$_2$ Solar Cells

We relied heavily on our routine characterization techniques such as Two-Probe and Three-Probe Current-Voltage (I-V) measurements, and Spectral Response. Variations were attempted in the fabrication procedure, and feedback was gained from the above techniques to correlate these variations to the performance of the devices. Wavelength-Dependent I-V, Capacitance-Frequency (C-F), Capacitance-Voltage (C-V), and $I_{SC}$-$V_{OC}$ measurements were done on selected samples from time-to-time, to gain knowledge about workings of specific regions of, or specific phenomena in, the solar cells.
4.4.1. Current-Voltage (I-V) Measurements

An HP 4145B Semiconductor Measurement Analyzer is utilized in either a 2-probe or a 3-probe configuration.

The 2-probe I-V measurement is the first measurement done on a completed solar cell device. The theory of I-V has been covered in the Background chapter. To measure one device out of the 25 device dots (defined by the ZnO mask), one probe is placed on the dot being measured, and the other probe is placed on the Molybdenum exposed (by scraping off the top layers) between the dots. The dark and the light (1-Sun intensity using a Solar Simulator) I-V curves for all 25 devices on a sample are obtained in this manner. Normally, this measurement provides the initial assessment of a sample, including the effect of any composition gradient effects. If the $V_{OC}$’s, $I_{SC}$’s, and the curve shapes are within the acceptable range, the next step is the 3-probe I-V measurement.

In the 3-probe set-up, two, instead of just one, probes are placed on the device dot (to touch the ZnO front contact layer). This is done so as to eliminate any contact (series) resistance effects, so that a more reliable measurement can be obtained. Because this measurement is cumbersome and time-consuming, all 25 devices from a sample are rarely measured. More often than not, one row and one column, or two rows and two columns, are measured. The FF’s can be calculated manually for each measured device by finding out the maximum power point. The $V_{OC}$ and the FF values from the 3-probe data are used, in conjunction with the $J_{SC}$ values from the Spectral Response (Quantum Efficiency) measurement, to calculate the conversion efficiency values for the solar cells.
4.4.2. Spectral Response

A Spex 4700 spectrometer is used to determine the external quantum efficiency (Q.E.) as a function of wavelength. The light source is calibrated using a Silicon Standard Cell Reference obtained from the National Renewable Energy Laboratory (NREL). The output, $J_{SC}$, of the cell at each wavelength is normalized against the Si reference to get the Q.E. versus wavelength curve. This curve is integrated against a reference AM 1.5 global spectrum to get the $J_{SC}$ of the device. The next figure depicts a representative Spectral Response curve.
4.4.3. Capacitance Measurements

Capacitance measurements can provide valuable information about the p-n junction, such as the depletion width, the doping densities and the doping profiles, and the built-in voltage.

The Capacitance-Voltage (C-V) measurement relies on the fact that the width of the depletion region varies with the applied voltage bias. The junction depletion region can be considered as a capacitor, with the capacitance per unit area given by

\[ C = \frac{\varepsilon}{W} \]  

(Eq. 4.1)
Where $\varepsilon$ is the dielectric constant of the semiconductor, and $W$ is the width of the depletion (space-charge) region.

If the doping densities of the p- and the n-side of the junction differ by more than two orders of magnitude, then the junction can be treated as a one-sided abrupt junction, with its entire depletion region lying on the lower-doping side. If this doping density is $N_A$, then the depletion width $W$ can be given by

$$W = \left[\frac{2\varepsilon_s (V_{bi} - V)}{qN_A}\right]^{\frac{1}{2}}$$  \hspace{1cm} (Eq. 4.2)

Where $q$ is the electronic charge, $V$ is the applied voltage, and $V_{bi}$ is the built-in junction voltage of the diode.

The capacitance can then be written as

$$C = \left[\frac{\varepsilon_s N_A}{2(V_{bi} - V)}\right]^{\frac{1}{2}}$$  \hspace{1cm} (Eq. 4.3)

Ideally, a plot of $1/C^2$ vs. $V$ should be a straight line, with a slope of

$$\frac{d\left(\frac{1}{C^2}\right)}{dV} = \frac{2}{q\varepsilon_s A^2 N_A}$$  \hspace{1cm} (Eq. 4.4)

The depletion width and the doping concentration can be calculated as follows.

$$W = \frac{\varepsilon_s}{C}$$  \hspace{1cm} (Eq. 4.5)

$$N_A = \frac{2}{q\varepsilon_s \text{ (slope)}}$$  \hspace{1cm} (Eq. 4.6)

Moreover, the x-axis intercept of this plot gives a value of the built-in voltage $V_{bi}$. 

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An HP 4194 Gain Phase Analyzer is used for our capacitance measurements. The I-V measurement that is done previously is used as a screening measurement to eliminate any devices that show obvious shunting in the 3-probe I-V plots. This is then followed by a Capacitance-Frequency measurement. Here, the frequency is varied from 100 Hz to 1 MHz. Typically, in the good devices, the capacitance signal is large at lower frequencies, but drops quickly to a lower value, and then saturates at this low value. Larger variations mean that the device is shunted, and such devices are not used for the following C-V measurement.

The C-V is carried out at a frequency of 500 Hz. This value is chosen because, at this frequency, the interface states or the stray capacitance from the leads and the set-up do not contribute to the measurement. The device is biased by applying a dc voltage $V$, which is varied from $-3.0$ to about $0.5$ Volts. A sinusoidal ac voltage of a small amplitude (about $10$ mV) is superimposed on the dc voltage. The plots for $C$ vs. $V$ and $1/C^2$ vs. $V$ are then obtained.

An example of a such a $1/C^2$ Vs. $V$ plot, obtained for a CIS solar cell, is shown on the next page [Karthikeyan, 1997]. As can be seen, the variation $1/C^2$ Vs. $V$ for this particular device is highly linear.
4.4.4. $I_{SC}$-VOC Measurements

When the mechanism of the junction transport differs from the ideal symmetrically doped p-n homojunction, a diode (ideality) factor $A$ is introduced in the basic equation for the junction current, which is reproduced below for convenience.

$$I = I_0 \left\{ \exp \left( \frac{q(V - IR_s)}{AKT} \right) - 1 \right\} - I_L + \frac{V - IR_s}{R_{sh}}$$

(Eq. 4.7)

Classically, the value of $A$ is between 1 and 2. However, an $A$ value greater than 2 has been observed in several studies, and this has been attributed to an asymmetry in the doping arising because of non-uniform spatial distribution of recombination centers at or near the junction interface [Bube, Photovoltaic Materials]. The diode factor, therefore,
can provide important information about the junction mechanisms in a solar cell. The $I_{SC}$-$V_{OC}$ technique is one popular method to calculate this factor.

Assuming that $R_{sh}$ is large enough so as not to affect the characteristic, the $V_{OC}$ can be given as (setting $I = 0$)

$$V_{OC} = \frac{AKT}{q} \ln \left[ \frac{I_L + I_0}{I_0} \right]$$  \hspace{1cm} (Eq. 4.8)

Recognizing that $I_L + I_0 \sim I_L = I_{SC}$,

$$V_{OC} = \frac{AKT}{q} \left[ \ln (I_{SC}) - \ln (I_0) \right]$$  \hspace{1cm} (Eq. 4.9)

And hence

$$\ln (I_{SC}) = \frac{q}{AKT} V_{OC} + \ln (I_0)$$  \hspace{1cm} (Eq. 4.10)

If a set of different $I_{SC}$ values and the corresponding $V_{OC}$ values can be obtained, they can be plotted as a straight line, and the value of $A$ can be derived from the slope of this line. It is possible to generate the set of values using neutral density filters. The $A$ values can then be correlated with the data from other measurement techniques, to gain valuable insights into the junction mechanisms.

An example of an $I_{SC}$ Vs. $V_{OC}$ plot, obtained for a CIS solar cell, is shown on the next page [Karthikeyan, 1997].
Figure 4.8. An $I_{SC}$-$V_{OC}$ Plot for a USF CuInGaSe$_2$ Cell [Karthikeyan, 1997]
CHAPTER 5.
RESULTS AND DISCUSSION

The results obtained for our CuIn(Ga)Se$_2$ and CuGaSe$_2$ solar cell devices will be presented and discussed in the following manner. Part I of this chapter will deal extensively with the processing results for CuIn(Ga)Se$_2$ and CuGaSe$_2$. In Part II, the modeling of our CuIn(Ga)Se$_2$ and CuGaSe$_2$ devices, carried out using two simulation techniques, will be discussed.

5.1. PART I: CuIn(Ga)Se$_2$ and CuGaSe$_2$ Processing Results

5.1.1. Relative Positions of the Substrate and the Sources

Before beginning the presentation of the results, here’s one important thing to remember: The discussion is, to a large extent, about the absorber deposition, and the effects of variations in the absorber recipe. Therefore, the relative positions of the substrate and the various sources (Cu, In, Ga and Se for CuIn(Ga)Se$_2$; Cu, Ga and Se for CuGaSe$_2$) play a crucially important role, in terms of the gradients of these elements in the final absorber film. For the reader’s convenience, the figure that depicts these relative positions is reproduced below.
Figure 5.1. Arrangement of the Substrate and the Sources

5.1.2. Ga Evaporation and the Sample-Numbering-System

During a single vacuum run, the four constituent elements, Cu, In (for CuIn(Ga)Se$_2$), Ga and Se, are deposited sequentially on a substrate, to accomplish the absorber layer deposition. Initially, a sputtering method was being used for the deposition of Ga, while the other constituent elements (Cu, In, Se) were deposited using an evaporation method. When this research project began, the above-mentioned Ga sputtering was still in use. With this process, for CuIn(Ga)Se$_2$, open-circuit voltages of the order of 425-450 mV had been achieved in our laboratory, with the short-circuit current densities exceeding 40 mA/cm$^2$. Later, however, it started becoming more and
difficult to control the sputtering and the evaporation systems in the same chamber, during a single run. The deposition uniformity on the substrate, as well as the run-to-run reproducibility, started getting affected. It was, therefore, decided that the sputtering gun for Ga be removed, and a Ga evaporation source be installed. For this, a few more changes had to be done to the internal geometry of the chamber. Consequently, our base process control was lost.

The next task, therefore, was to carry out the necessary calibrations and retrieve the base process. Around this time, with the new Ga evaporation, the sample # P001 was processed. All the samples that followed are numbered sequentially. The initial samples were CuIn(Ga)Se$_2$ devices. As a rule of thumb, unless otherwise specified, the samples until, and including, P033 were CuIn(Ga)Se$_2$ devices, whereas those beginning with P041 were CuGaSe$_2$ devices. (Samples P034 to P040 were an attempt to process CuGaSe$_2$-CuIn(Ga)Se$_2$ bi-layer devices, and these won’t be discussed here.)

5.1.3. CuIn(Ga)Se$_2$ Processing

As mentioned previously, a number of conclusions can been drawn on the basis of the I-V characteristics of various samples. In our study, some correlations have been observed, between the I-V parameters and the amounts/ratios of the elements deposited in the absorber layer. These will be discussed next, with the help of the results obtained for specific samples.
5.1.3.1. CuIn(Ga)Se$_2$ Sample # P020

Sample # P020 was one of the first CuIn(Ga)Se$_2$ samples, with the new Ga evaporation system, to exhibit a decent I-V performance. This sample had many devices that had open-circuit voltages of 400 and above, with the highest one at 425 mV. The following figure contains the data for the $V_{OC}$ of the 25 devices on this sample.

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<tr>
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Figure 5.2. Two-Probe $V_{OC}$ Numbers for CuIn(Ga)Se$_2$ Sample # P020

The following observations can be made from the above figures. First, with the exception of the two devices at the top right corner (the Cu-Se corner), the $V_{OC}$'s of all
the other devices are in the range of 385 mV to 425 mV. Typically, such a variation of performance is seen from one side of the substrate to the other side, and originates from the slight, but definite, variation in the ratios of the constituent elements. The two “bad” devices, with $V_{OC}$’s of 345 and 325, respectively, are the result of one or more of several possible effects, which are discussed next.

First, the occurrence of the low $V_{OC}$’s may be an outcome of a high (greater than 1.0) metal ratio (i.e. the ratio of Group I/Group III, or, in this case Cu/(In+Ga)). This is because these devices are closer to the Cu source, while at the same time being farthest from Ga, as well as In. At the first glance, it might seem rather strange that there is such a sudden drop in the $V_{OC}$’s for the two devices, while the two neighboring devices in the next row are 425 mV each. However, such an effect has been observed in a few other samples, where the devices with a metal ratio very close to 1 were the best among the lot, and as soon as the ratio went above 1, the performance dropped rather abruptly. This phenomenon, of Cu-rich devices being poorer in performance than their Ga- or In-rich counterparts, has often been discussed in the literature. The second possible cause for the above-mentioned low $V_{OC}$’s may be edge effects. It is possible that this corner of the sample was damaged, either during the handling or because of unwanted deposition effects such as masking because of the sample-holder. The third reason may be a poor-quality glass substrate piece, or even a non-uniformity produced during the Molybdenenum deposition. However, these reasons seem less likely than the first one, primarily because the rest of the sample shows very consistent gradients, and even the lesser performing devices show their own internal gradient -- the 325 mV device does, in fact, have a
slightly higher I/III ratio than the 345 mV device, making the I/III ratio the most likely cause of this behavior.

The figure on the next page shows the variation of the fill factors (calculated from 3-Probe I-V curves) with the change in position, for two rows of devices on this sample [Shankaradas, Thesis]. The four backside columns in this figure represent four devices from the third row: # 3, 8, 13 and 18, whereas the four front columns represent four devices from the second row: # 7, 12, 17, 22.

The following observations can be made from this figure. First, the FF numbers range from about 58% to about 50%, which is quite typical of our devices. Second, the FF performance is better towards the Se side of the sample, compared to the Ga side. A more-or-less similar gradient can be observed, for the two rows of devices, in the V_{OC} numbers. This is not surprising, as the V_{OC}’s and FF’s are often found to go hand-in-hand.

![Figure 5.4. Fill Factor Vs. Position of Device, for 8 Devices on Sample # P020](image-url)
A similar performance variation has been observed in other CuIn(Ga)Se$_2$ samples processed in this research. Some of these results will be presented later. It is reasonable to say that this may be the result of one of the following two reasons. First, it is possible that the amount of Se deposited was insufficient to the point that the Ga side of the substrate (the side opposite to Se) did not receive the amount of Se that it needed for the formation of the proper absorber phase. This can readily explain the above gradient in performance. However, this does not seem likely, as great care is usually taken to provide more than enough Se during the deposition process. The second, more likely reason could be that the Ga was responsible for the degradation of the devices. This could happen, for example, if the Ga deposited during the precursor layer deposition did not bond very well with the other elements. Such un-bonded Ga could produce defects in the material, thereby leading to the deterioration of the devices.

The above sample (# P020) had the following amounts of constituent elements deposited during the absorber precursor layer formation (as measured by the thickness monitors): 1360 A$^0$ Cu (this is called the Bulk Cu), 2900 A$^0$ In, 875 A$^0$ Ga, and about 45000 A$^0$ Se (this is the precursor Se, as against that deposited during the final selenization step). Also, towards the end of the selenization step, 30 A$^0$ of additional Cu (hereafter referred to as Top Cu) was deposited.

At this point, it should be noted that the above thickness numbers are not the actual numbers that get deposited on the substrate, and that there is a correction factor associated with it, depending on the distance of the source from the substrate. However, because these distances are constant from run-to-run, the correction factors are constant, too. Therefore, comparing the thickness numbers from the thickness monitors is quite
reasonable, and provides an easy way to track the run-to-run variations in the amounts/ratios of elements. (Typically, the variation in the thickness of a particular element across the sample was about 7-10 %.)

In an attempt to further understand the performance of our samples, the following experiments were undertaken, where the amounts and the ratios of different elements were systematically changed.

5.1.3.2. CuIn(Ga)Se$_2$ Samples # P030 and # P031

As mentioned previously, for our CuIn(Ga)Se$_2$ samples, Cu was deposited in two stages. Most of it was deposited early in the deposition sequence, in the precursor layer. This was called bulk Cu, as it was thought to participate in the formation of the bulk of the absorber layer. A very small amount, typically, about 30 to 50 Å, was deposited towards the end of the selenization stage. This top Cu was thought to play a key role in the formation of the surface layer of the absorber [Zafar, Dissertation].

Sample # P030 had 1350 Å of bulk Cu (as opposed to 1360 Å in # P020), whereas the top Cu was increased to 40 Å (from 30 Å of # P020). The total Cu amount essentially remained the same. The amounts of the other constituent elements were held constant. (The total Se amount during the precursor formation varied by about 10 %. However, as mentioned before, ample Se was usually available during the process. Moreover, much more extra Se was typically available during the selenization stage, to more than compensate for any possible deficiencies.) The $V_{OC}$ numbers for this sample are shown below.
Once again, a trend, of increasing $V_{\text{OC}}$ numbers towards the Cu side, can be noticed. This effect is even more pronounced than that in sample # P020. The higher $V_{\text{OC}}$’s are once again in the range of 415-425 mV, and are present in the first two rows, which are the rows closest to the Cu source. This indicates that a small change in the amounts of the top and the bulk Cu, while maintaining the same total amount, did not have much effect on the performance of the devices.

For the next sample, # P031, the bulk Cu was kept constant, while the top Cu was increased from 40 $\text{A}^0$ to about 55 $\text{A}^0$. The following $V_{\text{OC}}$ numbers were obtained.

| 235 | 365 | 205 | 365 | 365 |
| 365 | 375 | 375 | 345 | 365 |
| 355 | 335 | 295 | --- | --- |
| 395 | 375 | 335 | 305 | 335 |
| 375 | 375 | 355 | 355 | 355 |

It can easily be seen that the increase in the top Cu has had an overall detrimental effect on the performance of this sample. Although it looks like there might have been some other problems, as witnessed by the two dead devices depicted by “---“ and the poor performance in the area surrounding these bad devices, the highest voltage numbers have definitely shifted away from the Cu source (shifted down in the figure). This meant...
that 55 Å of Cu was too much, and, therefore, it would have to be cut back down. This conclusion has been corroborated by several other experiments with CuIn(Ga)Se$_2$ samples.

Keeping the above observations and conclusions in mind, we now turn our attention to CuGaSe$_2$ processing results.

An important thing to be noted is that CuGaSe$_2$ cells had been processed previously in our laboratory [D’Amico, Thesis]. The highest $V_{OC}$ and $J_{SC}$ values obtained in this research (on separate devices) were 675 mV and 14.3 mA/cm$^2$, respectively.

The results from the above CuGaSe$_2$ experience helped establish the starting point for the CuGaSe$_2$ project discussed in this document. However, as discussed before, because of an important modification to the existing deposition system (in the Ga deposition method), this project virtually began from scratch, by re-establishing the CuIn(Ga)Se$_2$ and CuGaSe$_2$ base processes. Therefore, the benefits of previous CuGaSe$_2$ experience were rather limited.

5.1.4. Type I CuGaSe$_2$

Calibration experiments were carried out to find out the equivalent amount of Ga to replace the In, for the formation of CuGaSe$_2$ absorber layers. Initially, the overall amounts of different elements were somewhat lower than those for CuIn(Ga)Se$_2$. Hence, the overall final thickness of the CuGaSe$_2$ absorber layer was less than that of a typical CuIn(Ga)Se$_2$ absorber (approximately 1.5 μm, instead of ~ 2 μm). The following description relates to the CuGaSe$_2$ processing experiments.
The first few results that are presented below relate to the Type 1 CuGaSe$_2$ process, which has been described in detail elsewhere. As a reminder, the recipe is reproduced below.

(i) Precursor Deposition (275 $^\circ$C):

a. *Initial* Ga evaporation, 100 A$^0$ (without any Se),

b. Ga and Se co-evaporation,

c. Cu evaporation.

(ii) Selenization (Se evaporation, a flux of ~ 28 A$^0$/s for about 28 minutes total):

a. Ramp up from 275 to 450 $^\circ$C,

b. 7 minutes at 450 $^\circ$C,

c. Ramp up from 450 to 550 $^\circ$C,

d. 7 minutes at 550 $^\circ$C (30-40 A$^0$ Top Cu optional),

e. Ramp down from 550 to 425 $^\circ$C,

f. Cool-down to room temperature, in vacuum (no Se during this phase).

In the following sections, we present the results for Type I CuGaSe$_2$ samples.

5.1.4.1. CuGaSe$_2$ Sample # P041 (Type I)

Sample # P041 was the first CuGaSe$_2$ sample to exhibit a $V_{OC}$ number higher than that obtained with CuIn(Ga)Se$_2$. Only one device, # 15, on this sample showed 505 mV, while all other $V_{OC}$ numbers were much lower. The precursors for this sample contained the following amounts of constituent elements:

(i) Cu: 1200 A$^0$ Bulk, 25 A$^0$ Top.
(ii) Ga: 100 A\textsuperscript{0} Initial, 4000 A\textsuperscript{0} Bulk.

(iii) Se (deposited with Ga precursor): 53 kA\textsuperscript{0}

(iv) Se (in the Selenization part): ~ 45 kA\textsuperscript{0}

The following table shows the $V_{OC}$ numbers for sample # P041.

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<tr>
<td>185</td>
<td>215</td>
<td>505</td>
<td>155</td>
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</tbody>
</table>

**Figure 5.7. Two-Probe $V_{OC}$ Numbers for CuGaSe\textsubscript{2} Sample # P041**

The appearance of a 500 mV device meant that the metal ratio (Cu to Ga ratio, in the case of CuGaSe\textsubscript{2}) was somewhere in the ballpark of what was needed. This ratio would now have to be adjusted so as to obtain more devices with better $V_{OC}$ numbers.

**5.1.4.2. CuGaSe\textsubscript{2} Sample # P042: Reduction in Cu**

In sample # P041, shown above, the only device that had 505 mV was located on the side opposite to that of the Cu source. This, then, indicated that the sample needed less Cu to be able to perform better. For the next sample, # P042, the amount of the bulk Cu was reduced from 1200 A\textsuperscript{0} to 1075 A\textsuperscript{0}, while the top Cu, deposited during the selenization stage, was maintained at 25 A\textsuperscript{0}. 

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As can be easily seen from the following table, many more devices showed $V_{OC}$’s in the range of 500 to 600 mV, with the highest one at 605 mV. It is, therefore, easily observed that the decrease in the amount of bulk Cu had helped the process. The higher $V_{OC}$ numbers were now centered on the middle of the sample, as regards the North-South direction (North is the Cu source side. Note that there is no In at the South, as we are dealing with CuGaSe$_2$ here, and not CuIn(Ga)Se$_2$.) However, in the side-to-side (West-East), i.e., the Ga-Se source direction, the improved devices seemed to be located towards the left side, which was nearer to the Ga source, and away from Se. A similar trend was observed for sample # P043, which is presented later.

Let’s now consider the variation in the $I_{SC}$ (current) numbers, as a function of the position of the individual device on the substrate, for sample # P042.

| 445 | 345 | 345 | --- | --- |
| 605 | 545 | 515 | 345 | --- |
| 545 | 555 | 535 | 425 | 195 |
| 525 | 545 | 525 | 365 | 445 |
| 305 | 245 | 325 | 455 | 335 |

**Figure 5.8. Two-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P042**

| .759 | .631 | .727 | --- | --- |
| .868 | 1.036 | .847 | .899 | --- |
| 1.119 | 1.132 | .869 | .570 | .534 |
| 1.048 | 1.123 | .990 | .884 | .716 |
| .958 | 1.015 | 1.006 | 1.009 | .684 |

**Figure 5.9. Short-Circuit Current ($I_{SC}$) Vs. Position of Device, for Sample # P042**
From the $I_{SC}$ Vs. position plot, it can be seen that the devices closer to the Se-Cu corner have poorer performance compared to those near the Ga side. An important thing to be noted here is that these $I_{SC}$ numbers depend on the areas of the individual devices. Because of the variations in the device areas (originating from the non-uniform ZnO contact deposition through the mask, to be described later), only limited conclusions can be drawn from this comparison. Nevertheless, this data can be taken as a general guideline. The main objective, throughout this project, had been to gain improvements in the $V_{OC}$’s. Therefore, much more emphasis was given to the $V_{OC}$ performance, than that of the $I_{SC}$’s. However, whenever warranted, the current-density ($J_{SC}$) numbers, which essentially eliminated the area-dependence, were used to compare the current-performance of the devices.

To be able to compare the trends in the $I_{SC}$ numbers, and eventually relate these trends to the absorber deposition parameters, another thing should be kept in mind. The current through the entire device structure also depends upon the quality of the top contact, which, in the case of our solar cells, was ZnO. As mentioned above, the active area of the device was defined by a mask during the ZnO deposition process. In this process, the ZnO sputtering target was located off-axis, towards one side of the substrate. Also, because of the substrate-holder arrangement during the CdS chemical bath deposition process (which precedes the ZnO deposition), the substrate had to be cut into two separate pieces. The geometry of the ZnO process could affect the devices in various ways. First, because of the angle involved in the masked ZnO deposition, shadowing effects originated. The areas (and, to a much lesser extent, ZnO thickness) of different devices were, therefore, different. Second, the two pieces (of the same initial substrate)
could receive slightly different amounts of ZnO, because of the fact that they were placed at two different corners of the ZnO substrate holder. The former effect was usually quite noticeable, while the latter had been proved to be negligible. A third effect, that was a consequence of the off-set target and the standard orientation used, was observed during the early stages of CuGaSe$_2$ development. Because there could be significant atomic/molecular bombardment during the ZnO sputtering process, the devices closer to the target may have faced significantly more damage than those farther away. This may have led to a gradient in performance. Such a gradient, arising because of ZnO variations, was in the East-West direction, the same direction for the gradient arising because of Ga-Se variations. This often complicated the analysis of the trends originating from the variation in the metal ratios. As a solution to this problem, a small change was introduced in the procedure, for all of the samples that were processed this point forward. The two pieces of a single sample (cut prior to CdS, and hence ZnO) were now arranged for the ZnO deposition in a way such that the bottom half was inverted with respect to the top half of the sample. This way, if there was a certain East-West gradient evident in the performance of the finished sample, the Ga-Se effect could easily be distinguished from the ZnO effect.

5.1.4.3. CuGaSe$_2$ Sample # P043: Continued Reduction in Cu

Because of the performance improvement that resulted from the reduction of the amount of Cu, it was decided to further reduce the bulk Cu, for the next sample (# P043). This sample had $1025 \text{ A}^0$ of bulk Cu (down from $1075 \text{ A}^0$), while the top Cu amount was
kept approximately the same (30 A$^0$, while the previous sample had 25 A$^0$, with an estimated inaccuracy of +/- 2 A$^0$). The following figure shows the $V_{OC}$ distribution for this sample.

![Figure 5.10. Two-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P043](image)

Although the number of devices with $V_{OC}$'s above 500 mV was smaller than that in the previous sample, most of these higher voltage devices were still located in a somewhat similar region of the substrate. The difference was that now there were two good devices (>500 mV) in the first row, which was closest to the Cu source. For the previous sample, the better devices were present in rows 2, 3, and 4, and there were none in the first row. This was to be expected, because the amount of Cu was lowered here, whereas there was no change in the amount of Ga or Se (East-West direction), compared to the previous sample.

Next, we present the data for the current ($I_{SC}$) values for sample # P043.

![Figure 5.11. Two-Probe $I_{SC}$ Numbers for CuGaSe$_2$ Sample # P043](image)
It can be seen that, except for a few corner devices, the $I_{SC}$ numbers for most devices turned out to be above 1 mA. Although there was some variation in these numbers, they were much more uniform than the past samples. A few devices from near the Ga-Cu corner were selected for the $J_{SC}$ measurement, to be carried out using the Spectral Response technique.

The following two figures depict the spectral response curves for devices #7 and 8 from sample P043 (these are the two devices with bold-faced current values above).

![Spectral Response Curve for CuGaSe$_2$ Sample # P043, Device # 7](image)

Figure 5.12. Spectral Response Curve for CuGaSe$_2$ Sample # P043, Device # 7
The $J_{SC}$ numbers, calculated from the above spectral response curves, were 14.8 mA/cm$^2$ and 15.2 mA/cm$^2$, for devices #7 and 8, respectively. This was very encouraging, because these current density values were close to the highest that could be expected of the CuGaSe$_2$ devices, with the theoretical maximum $J_{SC}$ predicted to be near 20 mA/cm$^2$. (However, as will be seen in the remainder of this report, it turned out to be impossible to further improve these $J_{SC}$ values.)

A couple of other important observations can be made from the above spectral response curves. First, the extrapolation of the drop in the curves near long wavelengths shows that the bandgap of this CuGaSe$_2$ material was around 1.63 to 1.64 eV. This was close to, but slightly less than, the theoretical bandgap value of 1.68 eV. This indicated
towards the formation of a material that was very close to the ideal CuGaSe₂ absorber material. On the short wavelength side, the response starts to drop around 420 to 430 nm. This is rather interesting, because this drop, which was present because of the absorption in the CdS window/buffer layer on the top of the CuGaSe₂, was expected to be around 500 nm. This indicated towards the presence of a very thin CdS layer, perhaps less than a 100 Å. It is possible that this layer was not a true CdS layer, but was rather present as an intermediate phase, or mixture, between CdS and the adjoining ZnO top contact layers. Such a material, with a bandgap value between the bandgaps of CdS and ZnO (2.4 eV and 3.2 eV, respectively), would manifest itself as a shift of the start of the drop to shorter wavelengths. The presence of such a layer could not be proved in this work, because of the lack of availability of certain advanced characterization techniques. (For example, such a layer could perhaps be identified with the help of Transmission Electron Microscopy.) However, simulation studies of our CuIn(Ga)Se₂ solar cells have indicated towards the possibility of such a CdS-ZnO intermixing [Shankaradas, Thesis]. Alternatively, the CdS layer could be a part of the space-charge (depletion) layer for the solar cell.

Another salient feature, which typically exhibited itself in all CuGaSe₂ spectral response curves, was the gradual decrease of the response in the long wavelengths- from about 600 nm, up to the bandgap-edge of 750 nm. This region was expected to represent the bulk of the absorber (as against the absorber surface). Therefore, such a drop may have been indicative of poor-quality absorber material in the bulk. One possibility was that a slightly different phase of the CuGaSe₂ material was present in the bulk, which decreased the absorption of the incident light. A second possibility was the presence of
structural defects in the bulk, either originating in the absorber itself, or propagating from the underlying Mo back contact layer, or even from the glass substrate itself.

5.1.4.4. Samples # P060, P061: Continued Reduction in Cu

We now turned our attention back to improving the $V_{OC}$'s of our CuGaSe$_2$ cells. The above samples had indicated that a reduction in Cu, and hence, a reduction in the Cu/Ga metal ratio, had helped improve the performance. It was, then, decided to continue to reduce Cu, until we saw a drastic reduction in the performance. This point, then, would define one extreme of the metal ratio. This happened at around 900 A$^0$ Cu, while the amounts of the other elements remained constant, with the metal ratio of about 0.85. It was found, along the way, that a Cu amount of about 950 A$^0$ seemed optimal, for the total thickness that was being used. The following table shows the $V_{OC}$ performance for sample # P060, which had 950 A$^0$ of bulk Cu, and 20 A$^0$ of top Cu.

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Figure 5.14. Two-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P060

It is clearly evident that the metal ratio adjustment helped improve the performance significantly. Several devices had $V_{OC}$'s over 600 mV, with one above 700 mV. The last row of devices, however, had suffered, either from the edge effects, or from a bad region of the starting substrate.
However, there are other places on this sample where the $V_{OC}$ was low, even if all the surrounding devices had higher numbers. Such non-uniformity could again be a result of low-quality substrate or a poor-uniformity of the Mo back contact deposition. These non-uniformities proved to be very difficult, even impossible at times, to track. Therefore, a decision was made to focus on increasing the highest $V_{OC}$ numbers, rather than worrying too much about such local fluctuations. Henceforth, we decided to track only those devices that had $V_{OC}$’s higher than 600 mV, as a measure of the $V_{OC}$ performance of the sample.

Sample # P061 had amounts of elements similar to what # P060 had. The following figure shows the $V_{OC}$ performance. Although there were (slightly) less number of devices with $V_{OC}$’s > 600 mV, the high $V_{OC}$ devices were located in the same region of the substrate. These numbers were still in the top row, with the highest one, once again, approaching 700 mV.

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<tr>
<th>620</th>
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Figure 5.15. Two-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P061

5.1.4.5. Sample # P063: Variation in the Initial Ga

All the above samples used an initial Ga layer of about 100 A$^0$. As a reminder, this initial Ga was the very first precursor layer deposited, before the Ga+Se co-evaporation. We decided to investigate the effect that this layer had on the performance.
The initial Ga thickness was reduced to 50 \( \text{Å} \) for one sample, reduced to zero for another, and was increased to 150 \( \text{Å} \) for yet another sample. The 150 \( \text{Å} \) sample, as well as the 0 \( \text{Å} \) sample exhibited a diminished performance. The sample with 50 \( \text{Å} \) initial Ga, sample # P063, had the following \( V_{\text{OC}} \)’s.

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</tbody>
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**Figure 5.16. Two-Probe \( V_{\text{OC}} \) Numbers for CuGaSe\(_2\) Sample # P063**

Two things can easily be noticed. The performance here was much more uniform, and almost all the \( V_{\text{OC}} \)’s were fairly high, with most of them above 650 mV. However, although more number of devices had voltages of > 600 mV, the highest number (of 685 mV) was, in fact, lower than that from the previous two samples, # P060 and P061 (705 mV and 695 mV, respectively). It was quite possible that, for this particular absorber thickness, a 50 \( \text{Å} \) initial Ga was more suitable. However, in the subsequent experiments, the total thickness of the absorber layer was increased, in an attempt to get away from the possible shunting effects in the absorber film, as well as, to reduce the occurrence of peeling of the absorber film. (Such a peeling was seen earlier to be resulting from deposition of Se, without a buffer layer such as the initial Ga layer.) For this increased thickness, a 100 \( \text{Å} \) initial Ga did, indeed, produce uniformity similar to what was seen above, along with improved \( V_{\text{OC}} \) numbers. The 100 \( \text{Å} \) initial Ga layer was, therefore, once again established as the first step in the absorber deposition process,
for our Type I samples. (Changing the thickness of the initial Ga layer did not
significantly affect the Type II samples.)

5.1.4.6. Samples # P062 and P082: I-V Curve-shapes and Absorber Thickness

All CuGaSe$_2$ samples processed until this time had fill factors in the range of
about 40%-50%. The following figure shows an example of a rather poor I-V curve,
drawn for device # 15 of sample # P062.

The following observations can be made from the figure. First of all, the curve in
the third quadrant, after the turn-on of the device, is far from being vertical. This usually
means that there is an unwanted series resistance in this sample, which bends the curve
away from the vertical. Although all practical devices will always have some finite series
resistance, the effect in this particular device is rather large. The series resistance in a
solar cell device generally comprises of the bulk resistance of the absorber material, and
any contact resistances that may be present. As the contacts used in this particular
structure are highly conductive, the resistance, more likely, is coming from the bulk of
the absorber material itself (although some contribution from the top contact ZnO is a
possibility). (The external measurement-contact-resistance is eliminated by using a third
probe on the top contact, during measurement.)
In the first quadrant (low reverse bias), an ideal I-V curve should be a horizontal line. The I-V curve presented above has a slight slope in this region. This may be the result of one or more of the following two reasons. Firstly, if there is shunting in the device, perhaps because of defects introduced during the deposition, this will bend the curve away from the horizontal. Alternatively, such a bend could occur because of poor collection of the photo-generated carriers. When the reverse bias increases, the collection improves, and hence the photocurrent slowly increases accordingly. This may happen because, with an increased reverse bias, the depletion region extends more into the bulk of the device, thereby increasing the number of carriers that can reach the depletion region and be collected on the other side.

To investigate the effect of shunting, and possibly reduce any shunting through the absorber layer, it was decided that the overall thickness of the absorber be increased.
Sample # P082 was processed in such a way that the absorber film was about 20% thicker than that in the past, while maintaining the same metal (Cu/Ga) ratio as before. The following table shows the $V_{OC}$ performance of this sample. (Unlike the previous $V_{OC}$ numbers, which were 2-probe, these numbers are 3-Probe numbers.)

<table>
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<th>659</th>
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<tr>
<td>457</td>
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<td>670</td>
<td>647</td>
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**Figure 5.18. Three-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample #P082**

As can be easily noticed, most of the $V_{OC}$'s are above 600 mV, with the highest one, Device #12, at 699 mV. The following figure, presented on the next page, depicts the 3-probe I-V curve plots for devices #11 and #12, with $V_{OC}$'s of 693 and 699, respectively.

A comparison of these next I-V curves to the one presented before (from # P062) indicates that, for this sample (# P082), the slope of the curve in the 1$^{st}$ quadrant is closer to the horizontal. It is reasonable to say that this is because of reduced shunting through the absorber layer, as only the thickness of the absorber was changed (increased) for this sample. Any change in the shunting or series resistance behavior of a device should show up in the squared-ness of the I-V curve in the 2$^{nd}$ quadrant of the 3-probe curve. Therefore, this reduction in shunting can be quantitatively measured in terms of the fill factor. Indeed, the two devices shown, from sample #P082, had substantially increased fill factors- 56% and 55%, for devices #11 and #12, respectively. The highest fill factor, for device #21, was 58 %, which resulted in a conversion efficiency of about 4.8%.
Figure 5.19. Three-Probe I-V Curve for Devices # 11, 12 for Sample # P082
5.1.5. Type II CuGaSe$_2$

As described in the literature survey, NREL researchers have used a three-stage recipe for the CuIn(Ga)Se$_2$ absorber preparation. In this recipe, the film starts out being Cu-poor, then goes through a Cu-rich phase (at a high temperature), and then goes back to being Cu-poor towards the end of the deposition. According to the literature, the intermediate Cu-rich phase helps form larger grains in the film, thereby improving the performance of the absorber.

We decided to explore such a Cu-rich-to-Cu-poor conversion for our CuGaSe$_2$ absorbers. The process that resulted was called the Type II recipe, and it went through the following deposition sequence.

(i) Precursor Deposition I (275 $^\circ$C):
   a. Initial Ga, 100 A$^0$,
   b. Approx. 4/5$^{th}$ part of (Ga and Se) co-evaporation,
   c. Cu.

(ii) Precursor Deposition II:
   a. Ramp up from 275 to 550 $^\circ$C (low Se flux),
   b. 10 minutes at 550 $^\circ$C (low Se flux),
   c. Remaining 1/5$^{th}$ part (Ga and Se) co-evaporation.

(iii) Selenization (Se evaporation, about 28 minutes total):
   a. 22 minutes at 550 $^\circ$C,
   b. Ramp down from 550 to 425 $^\circ$C,
   c. Cool down to room temperature (no Se during this phase).
In short, the (Ga + Se) layer, which was deposited all at once in the case of Type I, was now split into two layers. One of these (a major portion) was deposited before Cu, while the other after Cu, at high (550°C) temperature. One thing to be remembered about these Type II devices is that the Se amount used (i.e., evaporated) during the deposition was much higher than that normally used during a Type I process. This is because, for Type II, the substrate sat at a higher temperature for a much longer time. During this interval, if a constant low Se flux was not on, the Ga already present in the sample (from previous steps) might have left the sample, in the form of volatile Ga-Se species (this phenomenon is described before). Of course, it was also assumed that, although more Se was used, only that amount, which could combine with either Ga or Cu, or both, would be incorporated in the absorber film. (Such an assumption would not hold if the Se amount were excessively high.)

Let’s now look at some of the samples processed with this recipe. Initially, to be able to see whether the composition and structure of the Type II absorber is close to what we needed it to be, EDS and XRD characterizations were carried out on a sample. This characterization is discussed next.

5.1.5.1. EDS and XRD Characterization Results for Type II CuGaSe₂

Energy Dispersive Spectroscopy and X-Ray Diffraction were carried out on a CuGaSe₂ absorber film deposited on a glass substrate that was coated with Mo (Sample # P131, Type II CuGaSe₂). The EDS and XRD plots are included in Appendix 1 of this report.
EDS results showed that the ratio of the three (Cu, Ga, Se) elements present in the absorber layer was close to 1:1:2, which meant that the material was close to being CuGaSe$_2$. Because this was a standard-less EDS, another EDS scan was done on a CuGaSe$_2$ standard provided by NREL. The comparison between these two was used to derive the above conclusion. It should be remembered that EDS probes the top few thousand Angstroms of the material in question, and hence, the results are representative of the top portion of the film only. The deeper bulk material may have had a different ratio of elements, and hence a different phase, which would possibly give rise to a drop in the spectral response for longer wavelengths, as was discussed in the previous section.

XRD analysis showed that the structure of the analyzed CuGaSe$_2$ film was polycrystalline, with a preferred orientation along the [112] direction. This data is consistent with the recent data in the literature.

5.1.5.2. Type II Samples # P111, # P115: Effect of Se

For sample # P111, which was a Type II sample, the amounts of the individual elements were: 1080 A$^0$ Cu, 4400 A$^0$ Ga (4100 before Cu, and the remaining 300 after Cu). The following was the $V_{OC}$ performance.

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Figure 5.20. Three-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P111
Most of the $V_{OC}$’s are above 600 mV, with the highest one at 715 mV. One thing to be noted here is that the total Se amount could have been excessively large, when compared to the next sample that is presented below.

Sample # P115, which had similar numbers for Cu and Ga, had less Se (a deposition rate of 13 $\text{A}/\text{s}$, as opposed to 20 $\text{A}/\text{s}$, for the same period of time), during the first Ga-Se deposition step. Another change introduced was that the bottom piece of this sample (the bottom three rows) was annealed in air for 10 minutes, at 200 $^\circ$C, immediately after the CdS buffer was deposited. The top piece (top two rows) was the control piece, meaning that it was processed with a regular recipe, without any annealing. This was an attempt to see if an intermediate annealing, which had been claimed in some research papers to be helpful, would improve our devices as well. The following is the $V_{OC}$ performance of this sample.

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<td>695</td>
<td>755</td>
<td>765</td>
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</table>

|       | 495 | 715 | 595 | 505 | 555 |

Figure 5.21. Three-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P115

It can be seen, from the above figure, that the $V_{OC}$ performance of this sample is, in fact, better than that of the previous one. Two conclusions can be drawn from this result. Firstly, the reduction in the Se flux has helped the process (the top two rows). This has produced the highest $V_{OC}$ (non-anneal) seen so far in this research: 735 mV.
Secondly, in addition to the decreased Se, an air anneal after CdS also has helped improve the $V_{OC}$’s. (More about annealing in a later section.)

5.1.5.3. Type II Sample # P119: Initial Ga

For sample # P119, no initial Ga was deposited. The 100 Å reduction in the amount of Ga was compensated by increasing the Ga amount in the Ga+Se layer. The $V_{OC}$ performance was as follows.

\[
\begin{array}{cccccc}
425 & 705 & 665 & 685 & 685 \\
675 & 695 & 665 & 305 & 665 \\
675 & 695 & 635 & 645 & 685 \\
655 & 705 & 695 & 695 & 675 \\
625 & 605 & 725 & 705 & 505 \\
\end{array}
\]

Figure 5.22. Three-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P119

The above table clearly shows that the elimination of the initial Ga layer did not change the $V_{OC}$ performance significantly. This, in fact, points towards the possibility that the structure of a Type II absorber is quite different from a Type I absorber. This issue will be discussed in more detail in a later section.

5.1.5.4. Current Density Performance of Type II

Although improved $V_{OC}$’s, in general, were obtained with the Type II recipe, the $J_{SC}$ (current density) performance of these Type II samples was diminished. The next figure depicts the spectral response curve for device # 12 from sample # P115.
Figure 5.23: Spectral Response for CuGaSe$_2$ Type II Sample # P115, Device # 12
The $J_{SC}$ value calculated from this curve was 10.2 mA/cm$^2$. (As a reminder, the above device had a $V_{OC}$ of 725 mV.) Other Type II samples have consistently shown current density values in the range 10-11 mA/cm$^2$. Type I $J_{SC}$ values were generally higher by 2-3 mA/cm$^2$, ranging from about 12.5 mA/cm$^2$ to more than 15 mA/cm$^2$.

A number of experiments were carried out to improve the currents for Type II, but little success was achieved. This really points towards the basic structural difference between the two types of recipes. The very mechanism that lead to the improved $V_{OC}$’s seems to be the reason why the $J_{SC}$’s are lower in Type II devices.

5.1.5.5. Type II Sample # P132: Cu-rich $\rightarrow$ Cu-poor Transition

The main purpose behind designing the Type II recipe was to explore the possibility of a Cu-rich-to-Cu-poor transition in the absorber film. Although careful calibrations showed that the amounts of Ga deposited in the first and the last step (i.e., before and after Cu) would have carried the absorber film through this transition, it was deemed necessary to confirm this with some more experimentation.

For sample # P132, the thickness of the absorber layer was increased by about 7.5%. However, to make absolutely sure that the sample goes through a Cu-rich-to-Cu-poor transition, the increase in the Ga came only in the second Ga deposition (i.e., in the second Ga+Se layer, which comes after the Cu, at high temperature). This would, then, carry the absorber film through a transition from a metal ratio of about 1.05 to that of about 0.9. Following is the $V_{OC}$ performance of this sample.
Figure 5.24. Three-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P132

It can easily be observed that the sample performance is more uniform, in terms of the $V_{OC}$ numbers. (One easy way is to look at the minimum $V_{OC}$, which, in this case, is 595 mV, fairly close to being a 600 mV device.)

In addition to the above, the current density numbers were higher as well. The following table shows these $J_{SC}$ numbers for 9 devices on this sample. (Because of the time-consuming nature of this measurement, only a limited number of devices were measured.)

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<th>11.4</th>
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<th>12.1</th>
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<th>12.5</th>
<th>12.6</th>
<th>11.8</th>
<th>11.1</th>
</tr>
</thead>
</table>

Figure 5.25. Three-Probe $J_{SC}$ Numbers (mA/cm$^2$) for CuGaSe$_2$ Sample # P132

It can be concluded, from the results for # P132, that increasing the thickness of the absorber, while making sure that there is a Cu-rich-to-Cu-poor transition of the phases during the deposition, has helped form a better-quality absorber. It has been mentioned before that, according to the literature, such a transition helps form larger grains. If these larger grains are preserved until the end, it is understandable that the overall current density would be increased. This is because the current density changes as the grain-size
of the final film changes, especially if this size-increase is in the direction of the current flow. Moreover, the total increased thickness seems to have helped even-out the local fluctuations/differences, to produce a more uniform absorber film. This could have been a result of one or more of the following. First, because of the increased thickness, the surface of the absorber, which is supposed to play a crucial role in terms of the $V_{OC}$’s, is placed farther from the back contact as well as the glass substrate. This would, then, protect the surface from any non-uniformity originating in either the back contact or the glass substrate. Secondly, if there were any vertical shunting paths present (in the direction of current flow though the absorber film), perhaps because of pin-holes or metal particulates, an increased thickness may have helped keep these shunts away from reaching all the way through to the surface of the absorber. A third possibility is that, while increasing the total absorber thickness, the sample saw a longer period of high-temperature deposition, along with more amount of Se. These could have helped form a more uniform absorber, thereby evening out any possible fluctuations.

Until this point, it was clearly evident that Type II produced slightly better voltages, and more uniformity, but reduced current densities, when compared to Type I.

5.1.6. Type I-B and Type II-B CuGaSe$_2$: Cu-Se Co-evaporation

In an attempt to improve the $V_{OC}$’s and the overall performance, a small variation in the Type I and Type II recipes was explored. These two processes were, therefore, named as Type I-B CuGaSe$_2$ and Type II-B CuGaSe$_2$, respectively. In the regular Type I and Type II processes, Cu was evaporated alone, in the absence of any Se flux. In the I-B
and II-B processes, Cu was deposited along with a constant flux of Se. The primary motivation here was two-fold. First, we wanted to see if the Se flux helped in the making of a more uniform material, thereby improving the properties. Secondly, if there was any significant loss of Ga-Se species during the Cu deposition, the extra Se flux would help compensate for this loss.

Sample # P093 was processed using the Type I-B recipe. The following was the \( V_{OC} \) performance of this sample.

\[
\begin{array}{cccccc}
645 & 715 & 705 & 665 & 725 \\
665 & 715 & 645 & 715 & 725 \\
665 & 675 & 635 & 625 & 615 \\
665 & 655 & 645 & 505 & 665 \\
405 & 545 & 605 & 625 & 445 \\
\end{array}
\]

**Figure 5.26. Two-Probe \( V_{OC} \) Numbers for CuGaSe\(_2\) Type I-B Sample #P093**

The highest \( V_{OC} \) was improved to 725 mV. The rest of the sample also had a decent performance; with most devices exhibiting \( V_{OC} \)’s greater than 600 mV.

Sample # P151 was a Type II-B sample (Cu-Se co-evaporation), with the following performance.

\[
\begin{array}{cccccc}
455 & 445 & 565 & 715 & 715 \\
695 & 675 & 725 & 735 & 725 \\
715 & 715 & 655 & 725 & 695 \\
665 & 715 & 695 & 715 & 705 \\
705 & 695 & 695 & 615 & 655 \\
\end{array}
\]

**Figure 5.27. Two-Probe \( V_{OC} \) Numbers for CuGaSe\(_2\) Type II-B Sample #P151**
It can be easily seen that the highest $V_{OC}$ (735 mV) is as high as the best numbers found with any other Type I or Type II samples. Interestingly, this sample also has the maximum number of 700’s so far -- 12 devices. These 12 devices are fairly scattered across the entire substrate, indicating that the metal ratios across the entire substrate are not very far from each other (or, at least, not far enough so as to diminish the $V_{OC}$ performance significantly).

A couple of conclusions can be drawn from the above two pieces of data. First, for both, Type I as well as Type II, the Cu-Se co-evaporated samples (The B Type samples) are better than the regular-recipe samples. This means that the Cu-Se co-evaporation works (at least) slightly better than the Cu evaporation, in terms of improving the $V_{OC}$ performance. Second, Type II-B seems to be better than Type I-B. This is mainly evident in terms of the uniformity on the substrate (many more 700’s for Type II-B, and they are scattered over a larger region of the sample).

The problem with this Cu-Se co-evaporation recipe, however, was that it was extremely difficult to control the amount of Cu in the samples. The reason was as follows. Because of the geometry of the sources in the CuGaSe$_2$ deposition chamber, and because of the high flux of Se that was always used during the Ga+Se co-evaporation step, the inside of the chamber usually got coated with Se. Some of this Se inevitably found its way on to the Cu source (a tungsten/tantalum boat that held the Cu pieces), in spite of the presence of a small separator-shield between the Se and Cu sources. In the regular Type I and II recipes, it was fairly easy to get rid of this Se sitting in and around the Cu boat, by heating up the Cu source before the substrate was exposed to the Cu evaporation (by opening the substrate shutter only after this Se had evaporated).
However, during the Type B processes, because Cu and Se had to be evaporated simultaneously, it was extremely difficult to decide how much of the material coming from the Cu source was indeed Cu, and how much of it was extra Se that might have been bouncing off the hot surfaces around the Cu boat. Because of this limitation, although slightly higher voltages were obtained, the Type B recipes could not be continued.

5.1.7. CdS and Other Buffer Layers

At this point, it was evident that, no matter what we did to the absorber, the $V_{OC}$, which was the main parameter we were trying to improve, was limited to the low 700’s. For the device characteristics, the next important layer, in the CuGaSe$_2$ solar cell structure, was the CdS buffer layer, along with the i-ZnO layer. We turned our attention to these two layers.

As mentioned in the literature survey, CdS has worked out best, as the buffer layer for CuIn(Ga)Se$_2$, as well as for CuGaSe$_2$. In our laboratory, a chemical bath deposition (CBD) of CdS had always been used as the standard buffer layer. (As a reminder: this CdS layer is usually followed by a thin layer of undoped ZnO, and then a much thicker layer of the top contact, viz. doped ZnO.) It is, perhaps, important to mention here that this CBD-CdS is one of the least understood steps in our processing sequence. Because our CuGaSe$_2$ recipe had evolved over time, it was warranted to carry out experiments that would tell us if CdS was, indeed, the best buffer layer for our
devices, and, if it was, then it needed to be seen if we could, somehow, optimize the CdS process for our CuGaSe$_2$ recipe.

At this point, it is important for the reader to be aware of some details of our CBD process. The process typically began with a mixture of 150 ml water and 27.5 ml Ammonium Hydroxide (1 Molar), which was then heated slowly, while being stirred. When the mixture reached 30$^\circ$C, the sample was placed in this solution, and 22 ml each of Cadmium Acetate (0.015 Molar) and Thiourea (0.15 Molar) were added. When the solution/sample temperature reached about 74-75$^\circ$C, the solution typically started turning yellow, because of the sulfur-containing precipitation. About a half minute or so later, at about 77$^\circ$C, the sample was taken out of the solution, rinsed, and blow-dried.

Meanwhile, it is also worthwhile to recall an important piece of information from the recent literature, where the best CuGaSe$_2$ performance so far was accomplished by tweaking the CBD-CDS process, by raising the CdS precipitation temperature to about 80$^\circ$C [Rau, et al.]. This information was used in designing the last two of the experiments described below.

To see how the CdS process affected our devices, we set out by processing a sample where we skipped the CdS layer completely. Not surprisingly, this sample turned out to be ridiculously low in performance. We then carried out a series of experiments where we used the following processing variations, one-by-one, with the Type I CuGaSe$_2$ absorber recipe:

(i) A double CdS layer was deposited, where the entire sequence of a CBD deposition was repeated. The performance was very poor.
(ii) A set of experiments involved samples that were heated outside, independently of the CdS bath, and immersed in the solution directly at various stages of the precipitation (in the range of 74-78°C). The performance was still quite poor.

(iii) The sample was taken out approximately at the point where the solution would start turning yellow (74°C). The sample, hence, was thought to have a thinner CdS layer in this case. The performance was as good as a standard CdS process, in terms of the voltages and currents.

(iv) The amount of Thiourea was increased by about 25% for a sample. This resulted in a poor performance.

(v) In order to raise the precipitation temperature, the sample was heated outside to about 88°C, and then immersed in the CdS bath, at about 75°C. The exact temperature of the sample at the time of precipitation could not be known, although, it had to be somewhere between the two temperatures stated above. The performance was low, and there were a number of small particulates on the sample.

(vi) In order to raise the precipitation temperature, the amount of Ammonium Hydroxide was significantly increased (approximately doubled). The precipitation temperature was raised to 80°C, and the sample showed good V_{OC}’s. However, the currents were extremely low, indicating that the absorber was attacked severely by the chemicals.

It can be seen, from the above list, that many of the experiments did not produce good performance. In the very last experiment, although the CuGaSe$_2$ precipitation could be increased to 80°C, there were other problems, and, hence, this direction of investigation was abandoned (in favor of other things).
It is interesting to note, however, that the third experiment in the above list, where the sample was taken out of the CdS bath rather prematurely (before the precipitation began), yielded excellent results. Most of the devices on this sample exhibited a $V_{oc}$ of $>600$ mV. Moreover, the $V_{oc}$ numbers were more evenly spread-out, indicating that this sample was better in terms of the uniformity. This was an important result in two ways. It was thought (at least in our laboratory) that the precipitation stage was crucially important in terms of forming the much-needed buffer layer on the absorber film. Secondly, it was known, from past literature, that the CdS bath also passivated the absorber surface, thereby reducing the possibility of interface defects. It was not known when this passivation exactly occurred, or when the passivation was completed, during the CdS process. From the above experiment, it could be concluded that the passivation was completed around the time the precipitation began. It is possible that, in the experiment, the precipitation had actually begun, but wasn’t quite visible yet, when the sample was taken out. In any case, it is reasonable to say that either the necessary CdS layer was formed before significant precipitation occurred, or a thinner CdS layer was actually sufficient for the sample. Because of practical limitations, we were unable to find out which one of these was the case. Also, taking the sample out of the bath before a significant amount of precipitation occurred resulted in better uniformity, suggesting that leaving the sample in the solution for too long may hurt the sample.

At this point, we decided to try out other buffer layers as possible replacements for the CBD-CdS layer. A number of other layers, such as evaporated Gallium Selenide ($\text{Ga}_2\text{Se}_3$)- with and without a vacuum break, evaporated Indium Selenide ($\text{In}_2\text{Se}_3$), a CdS layer followed by another layer of evaporated $\text{In}_2\text{Se}_3$, evaporated Zinc Indium Selenide
(ZISe), and a CdS layer followed by evaporated ZISe, were attempted. Along with some of these experiments, the i-ZnO layer thickness was varied, to see the effect on the properties of the devices. None of these new buffer layers worked nearly as good as the CBD-CdS. Therefore, the results are not presented here. CBD-CdS, as the prevailed winner, was continued as the buffer layer of choice.

5.1.8. Light-Soaking and Annealing Experiments for CuGaSe$_2$

To better understand the characteristics of our CuGaSe$_2$ samples, we decided to explore the effects of Light-Soaking and high temperature annealing. Some of the CuGaSe$_2$ samples were light-soaked under one-sun illumination, for about 10 minutes. A three-probe I-V measurement was then carried out on selected devices, after letting the soaked sample cool down for about 30 minutes. The measurement was then compared with that before the light-soaking (i.e., the as-deposited measurement). Some of the samples were annealed in air, at two different temperatures: Anneal #1 at 125$^\circ$C, and Anneal #2 at 200$^\circ$C. Some other samples were annealed only at the higher temperature (200$^\circ$C). The results obtained are discussed next.

Sample # P098 was processed with a Type II CuGaSe$_2$ recipe. The following figures (shown on the next 2 pages) depict the three probe curves for device # 6 on this sample. The four figures show the three-probe I-V curves for the device at 4 different times: As-deposited, after light-soak, after the 1$^{st}$ anneal, and after the 2$^{nd}$ anneal.
Figure 5.28a. Three-probe I-V for P098-06: As-dep/Light Soak
Figure 5.28b. Three-probe I-V for P098-06: Anneal-1/Anneal-2
The following observations can be made from these plots. First of all, the $V_{OC}$ progressively changed from 571 to 600, to 616, to 660. This means that the light soak has had some effect on the device, increasing the $V_{OC}$ by 29 mV. The first, low-temperature ($125^\circ C$) anneal improved the $V_{OC}$ by another 16 mV, whereas the second, high-temperature ($200^\circ C$) anneal increased it by 44 mV. We will compare this $V_{OC}$ behavior to another set of 4 figures, which are for another device from the same sample.

However, before that, there is another thing that can be noticed in the above plots. The very first (as-deposited) curve shows some amount of crossover of the dark and the light curves, in the 3\textsuperscript{rd} quadrant of the graph. This (unwanted) behavior has been seen in a number of CuGaSe$_2$ (and CuIn(Ga)Se$_2$) samples, to various degrees. The worst (maximum) crossover we have seen seems to be present in samples where the ZnO deposition process had problems. An example of such problems is: the sample going through an extra heating cycle before the ZnO deposition, because the run had to be shut down due to problems with gas pressures or the ZnO target. It is quite possible that, because of such oddities in the processes after the absorber deposition, either the junction interface and/or the top layer of the absorber got disturbed, perhaps leading to additional defect formations, which showed up as crossovers in the I-V characteristics. The amount of this crossover is almost equal for the first two plots, then it increases some, in the 3\textsuperscript{rd} plot (this is rather hard to see because of the changed scale), and increases substantially in the 4\textsuperscript{th} plot. This seems to indicate that, for a sample that had some crossover to begin with, the light-soaking has a small effect, whereas the annealing, especially the one at high-temperature, seems to have a substantial effect.
We now turn our attention to another device, # 24, from Sample # P098 (the same sample as above). The following four figures (on the next two pages) show the behavior of this device before and after light-soaking and annealing, just like the previous set of figures.

In this case, the $V_{OC}$ started out at 520 mV, then decreased by 12 mV after the light-soaking, and increased by 3 mV after the first anneal. Up until this point, the change was rather small. However, when the sample was annealed at a high-temperature, the $V_{OC}$ increased by 31 mV.

Comparing the above observations to the results of the previous device, the main difference seems to be the behavior after the light-soaking. In the previous case, the $V_{OC}$ increased after the light-soaking, whereas, here, it decreased a little. In fact, after carrying out similar study on a number of other samples, it became evident that the $V_{OC}$ fluctuated in both directions after light-soaking, and there was no unique, common trend. However, it became very clear, that the annealing, especially the high-temperature (200°C) one, always resulted in substantial increases in the $V_{OC}$ numbers.

It is also interesting to note that, just like the previous device, this device shows changes in the crossover phenomenon. Although the device started out with a minimal crossover, which remained fairly constant after the light-soak, it became worse after the first anneal, and the second anneal deteriorated it drastically. We’ll analyze the annealing behavior more, with the help of a few more examples.
Figure 5.29a. Three-probe plots for P098-24: As-dep/Light Soak
Figure 5.29b. Three-probe plots for P098-24: Anneal-I/Anneal-2
Let us, now, look at the annealing results for another sample, # P082. Unlike the previous one, this was a Type I CuGaSe$_2$ sample. The $V_{OC}$ results for this sample were presented in the CuGaSe$_2$ Type I section. At that time, it was also mentioned that device #12 from this sample had a decent fill factor, of 55%. The sample was later annealed at 200$^\circ$C, and the following figures show the before-anneal and after-anneal results for device #12.

Figure 5.30a. Three-probe for Sample # P082, Device # 12: As-dep
From the above figures, it can again be seen that the annealing has improved the $V_{OC}$, from 699 mV to 714 mV. Although this increase was rather small, compared to the increases seen in the $V_{OC}$’s for devices from the previous sample, it has to be remembered that the starting $V_{OC}$ (699 mV) was much higher in this case. The increase in this case was probably limited by another mechanism controlling the interface properties. It should also be recalled that the high $V_{OC}$ limit experienced with Type I samples is lower than that experienced with Type II samples. Because the sample in question is a Type I sample, with a $V_{OC}$ as high as 699 mV, it probably already was closing in on the limit, and therefore, the $V_{OC}$ improvement was limited.
Another interesting observation that can be made from the above figures is that, as the $V_{OC}$ increased because of the high-temperature annealing, the $I_{SC}$ has actually gone down, from about 1.16 mA to about 0.73 mA. This behavior has been quite representative of the annealed samples, meaning that the $I_{SC}$ always seemed to go in the opposite direction of the $V_{OC}$. This is rather discouraging, because this meant that the $V_{OC}$ and the $I_{SC}$ behaviors could not be separated, and hence, could not be improved independently of each other. However, this behavior seems to be consistent with the fact that, while the best $V_{OC}$’s obtained with the Type II recipe are higher than those obtained with Type I, the $I_{SC}$’s (and the $J_{SC}$’s), are, in fact, lower. One primary difference between the two recipes is that the Type II absorber is exposed to a higher temperature for a much longer period of time. This indicates to an effect of longer periods of high temperature on the absorber properties. Although the recipe change relates directly to the formation of the absorber, whereas the annealing could be thought of only re-arranging the absorber or the interface, both do involve the application of temperature over long periods of time.

Another experiment was attempted, where a sample was annealed in between the depositions, unlike the above samples, which were annealed after all the depositions were completed. The sample was # P115, and was presented in the Type II section before (although, the annealing wasn’t discussed in detail). The bottom piece of this sample (the bottom three rows) was annealed in air for 10 minutes, at 200 0C, right after the CdS buffer was deposited. The top piece (top two rows) was the control piece, meaning that it was processed without any annealing. This was an attempt to see if an intermediate annealing, which had been claimed in some research papers to be helpful, would improve our devices as well. The following was the $V_{OC}$ performance of this sample.
Figure 5.31. Three-Probe $V_{OC}$ Numbers for CuGaSe$_2$ Sample # P115

The top two control rows contain devices that have $V_{OC}$’s of 735 and 725, the two highest numbers seen for our regular (non-treated) CuGaSe$_2$ processing. What is even more interesting is that the bottom three rows, which were annealed after CdS, produced $V_{OC}$ numbers as high as 775 mV! This number was the highest of all samples produced (treated or non-treated) in this research project. It is possible that the annealing helped the CuGaSe$_2$-CdS interface properties by passivating it better, by activating some kind of diffusion mechanisms, whereby, ions traveled into the absorber to reduce the defect density present at or near the interface. Such a defect reduction would then result in the reduction of the dark current, thereby producing a higher $V_{OC}$.

5.1.9. Capacitance Studies of CuGaSe$_2$

To gain more understanding about characteristics such as the nature of the junction formed in the CuGaSe$_2$, the depletion width, and the doping concentration, we decided to study the capacitance behavior of our samples. Typically, a Capacitance-Frequency curve was obtained for several devices on a sample, as a screening mechanism. On a few good devices, a dark C-V and a light C-V measurement was carried out. This procedure has been described in detail in a previous chapter.
Sample # P082 was a Type I sample that yielded decent performance, and the I-V characteristics of this sample have been described in detail before. A few devices on this sample were then selected for the C-V measurements. The following figure shows the $A^2/C^2$ vs. $V$ curves (dark and light) for device # 1 on this sample. ($A$ is the area of the device, $C$, the capacitance, and $V$, the voltage applied.)

![Graph showing $A^2/C^2$ vs. $V$ for device #1 on CuGaSe$_2$ Sample # P082](image)

**Figure 5.32. $A^2/C^2$ Vs. $V$ Curve for Device # 1 on CuGaSe$_2$ Sample # P082**

As can be seen in the figure, the dark curve and the light curve do not overlap. We have seen this behavior with all of our CuGaSe$_2$ devices, as well as the CuIn(Ga)Se$_2$ devices processed in our laboratory [Jayapalan, et al.]. The underlying mechanism for the increased capacitance in light has been known to be the trapping of light generated carriers, which results in the change in the width of the space-charge (depletion) region [Shankaradas]. In the case of our CuIn(Ga)Se$_2$ devices, these traps have been correlated...
to recombination centers that seem to influence the $V_{OC}$ of the devices [Jayapalan]. It is evident that such traps are present in our CuGaSe$_2$ devices as well. However, attempts to find out a correlation between them and the $V_{OC}$ were unsuccessful.

The calculation of the depletion width in dark and light, in the above case, yielded the values of 617 and 515 Å$^0$, respectively. To find out the doping concentration, a slope value is needed, from the $A^2/C^2$ Vs. V curve. For this purpose, the near-flat region of the curve, from –1.5 Volts to 1.0 Volts, was selected. This is primarily because, at lower voltages (less reverse bias), the capacitance value may be affected by the forward capacitance. The following figure reproduces these selected regions of the above curves, along with the linear equations derived by curve fitting.

![Figure 5.33. Truncated $A^2/C^2$ Vs. V Curve for Device # 1 on Sample # P082](image)

For the above device, the doping concentration was calculated to be 5E15/cm$^3$. This value agreed with another device from the same sample. Most of the devices
yielded the values in the range of 1E15 to 5E15/cm³, with the exception of one device, which had a value as high as 6E16. (This particular device seemed to have an unusually small depletion width, as discussed later.)

According to the theory of the C-V measurement, the extrapolation of the straight-line C-V curve to the voltage-axis is supposed to yield the built-in voltage for the device. In the above case, it can be seen that such an extrapolation would give a value of about 2 Volts. A few other devices on this sample had a similar behavior. This, obviously, is too high to be the real built-in voltage. This may be a result of the inaccuracy originating from any shunting that may be present in these devices, thereby limiting the usefulness of the measurement itself.

Similar measurements were done on a few other selected samples. Sample # P082, presented above, was processed with a Type I CuGaSe₂ recipe. Another sample, # P115, was a Type II sample. A third sample selected, P093, was processed with a Type I-B recipe. As a reminder, the B type recipes included a low Se flux while the Cu was being deposited. The primary motivation behind this variation was two-fold. First, we wanted to see if the Se flux helped in the making of a more uniform material, thereby improving the properties. Secondly, if there was any significant loss of Ga-Se species during the Cu deposition, the extra Se flux would compensate for this loss.

C-V measurements were carried out on several devices from the above 3 samples, and the following figure presents the dark-depletion-width values (in Angstroms) for these devices. (The devices came from various locations from a sample, and the x-axis merely represents the number of device, not to be confused with the number representing the location with respect to the sources.)
Keeping the limitedness of the measurements in mind, a couple of important observations can be made from the above figure. First, there is a large variation among the depletion width values of devices from sample # P082. The values range from about a 100 to over 2000 Å. The smallest value of depletion width corresponded with the device that showed a high doping concentration of 6E16 before. However, four of the seven values are around 500 to 700 Å, and it seems likely that this is a good indication of where the true values may be. This is possible, especially because the variation in the values for devices from the other two samples is much smaller. For sample # P093, the values are between 100 and 200 Å, while those for sample P115 are mostly between 30 to 50 Å. Although all of these values (especially for # P093 and # P115) are too low compared to some of the values we have previously seen with our CuIn(Ga)Se$_2$ samples (several hundred nanometers), there is a trend that can be observed. As a reminder, Type I devices always had better current performance than Type II devices, and it is reasonable...
to see Type I depletion widths to be larger than those of Type II devices. Therefore, in the present case, it is no surprise that both, Type I (P082), as well as Type IB (P093), samples have better depletion widths than the Type II sample (P115).

5.2. PART II: CuGaSe\textsubscript{2} Simulation/Modeling Results

Even after a number of processing experiments, the V\textsubscript{OC}’s of our CuGaSe\textsubscript{2} devices were still limited to about 700-800 mV. To be able to better understand this performance limitation, we decided to employ two simulation techniques- SCAPS and AMPS- to model the device behavior. The primary motivation was to see whether the problem existed at the heterojunction interface, or in the deep absorber bulk, or at the back contact. The following sections describe selected results from this study.

5.2.1. SCAPS Modeling

The first technique, called Solar Cell CAPacitance Simulator (SCAPS), was developed by Prof. Marc Burgelman and his colleagues at University of Gent, in Belgium. The technique had previously been used to model CdTe and CuIn(Ga)Se\textsubscript{2} solar cells. For our simulations, we used the SCAPS-1D, version 2.1, which was the latest version available at the time.

First, a little bit about the SCAPS technique. The program simulates the electrical characteristics for thin film heterojunction solar cell structures. An arbitrary number of semiconductor layers, with arbitrary doping profiles (as a function of position) and
arbitrary energetic distributions of deep donor and/or acceptor levels can be introduced in the semiconductor bulk or at the heterojunction interface, and the effects of these can be observed in the electrical characteristics such as I-V, C-V, etc.

For our simulation purposes, we focused on the I-V behavior of CuGaSe$_2$ solar cell structures. We used the following typical values for the various parameters, unless otherwise specified later in the discussion.

**Table 5.1. SCAPS Simulations: Layers and Typical Parameter Values**

<table>
<thead>
<tr>
<th>Layer #</th>
<th>Layer Function in structure</th>
<th>Parameter name</th>
<th>Parameter value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Back contact (Moly)</td>
<td>Work function</td>
<td>4.80</td>
</tr>
<tr>
<td>2</td>
<td>Absorber (p-type) (CuGaSe$_2$)</td>
<td>Thickness</td>
<td>1.5 µm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bandgap</td>
<td>1.68 eV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Affinity</td>
<td>3.32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Acceptor density</td>
<td>1E+17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Absorption constant</td>
<td>1E+5</td>
</tr>
<tr>
<td>3</td>
<td>Heterojunction partner (CdS)</td>
<td>Thickness</td>
<td>550 Å</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bandgap</td>
<td>2.42</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Affinity</td>
<td>4.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Donor density</td>
<td>1E+14</td>
</tr>
<tr>
<td>4</td>
<td>Buffer layer (i-ZnO)</td>
<td>Thickness</td>
<td>550 Å</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bandgap</td>
<td>3.45</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Affinity</td>
<td>3.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Donor density</td>
<td>1E+16</td>
</tr>
<tr>
<td>5</td>
<td>Front contact (ZnO)</td>
<td>Work function</td>
<td>3.7</td>
</tr>
</tbody>
</table>

A number of simulation runs were carried out, where various defect levels and defect densities were introduced in the absorber bulk and/or at the interface between the
absorber and the heterojunction partner. The following pages contain the summary of these simulations.

The table below has information about simulations where there were only interface-defects present (no bulk-defects). The first column denotes the file name, i.e. the name of the simulation run. The next column has the information about the type, density, and location (from the valence band) of the interface defects. The last four columns show the results obtained for the respective I-V simulation, in terms of the $V_{OC}$, the $J_{SC}$, the fill factor, and the conversion Efficiency. (Note: The very first run had no defect-states at all, and is, therefore, named as J_base, meaning the base-run)

Table 5.2. SCAPS Simulation Parameters and Results: Interface-States Only (No defects for J_base, the first row)

<table>
<thead>
<tr>
<th>File name</th>
<th>Interface defects</th>
<th>$V_{OC}$, Volts</th>
<th>$J_{SC}$, mA</th>
<th>FF, %</th>
<th>Eff, %</th>
</tr>
</thead>
<tbody>
<tr>
<td>J_base</td>
<td>No defects</td>
<td>1.28</td>
<td>14.36</td>
<td>69.0</td>
<td>12.65</td>
</tr>
<tr>
<td>J_i1_1</td>
<td>Neutral/ E12/ 0.60</td>
<td>0.486</td>
<td>14.32</td>
<td>70.2</td>
<td>4.88</td>
</tr>
<tr>
<td>J_i1_2</td>
<td>Donor/ E12/ 0.60</td>
<td>0.380</td>
<td>14.49</td>
<td>61.1</td>
<td>3.36</td>
</tr>
<tr>
<td>J_i1_3</td>
<td>Acceptor/ E12/ 0.60</td>
<td>0.487</td>
<td>14.32</td>
<td>70.1</td>
<td>4.89</td>
</tr>
<tr>
<td>J_i1_6</td>
<td>Neutral/ E12/ 0.40</td>
<td>0.485</td>
<td>14.33</td>
<td>70.2</td>
<td>4.88</td>
</tr>
<tr>
<td>J_i1_7</td>
<td>Donor/ E12/ 0.40</td>
<td>0.383</td>
<td>14.40</td>
<td>63.5</td>
<td>3.50</td>
</tr>
<tr>
<td>J_i1_8</td>
<td>Acceptor/ E12/ 0.40</td>
<td>0.488</td>
<td>14.29</td>
<td>70.5</td>
<td>4.91</td>
</tr>
<tr>
<td>J_i1_9</td>
<td>Neutral/ E12/ 0.20</td>
<td>0.522</td>
<td>14.36</td>
<td>77.0</td>
<td>5.77</td>
</tr>
<tr>
<td>J_i1_10</td>
<td>Donor/ E12/ 0.20</td>
<td>0.513</td>
<td>14.36</td>
<td>78.3</td>
<td>5.77</td>
</tr>
<tr>
<td>J_i1_11</td>
<td>Acceptor/ E12/ 0.20</td>
<td>0.554</td>
<td>14.11</td>
<td>77.5</td>
<td>6.05</td>
</tr>
</tbody>
</table>

The following figure shows the light I-V graphs drawn for some of the above simulation runs, viz. J_base, J_i1_1, 2, 9, 10, and 11.
A couple of important observations can be made from the results of this set of simulations. Firstly, the J_base run, where there were neither bulk-states nor interface-states introduced, produced a $V_{OC}$ of 1.26 Volts, with current and FF values of 14.36 mA/cm$^2$ and 69%, respectively. Because the aim was to simulate a device as close to our processed devices as possible, we had to introduce defect-states so as to bring this simulated $V_{OC}$ down. A series of runs, where there were different types of interface-defect-states introduced at different locations from the valence band edge, all with the
density of 1E12, brought this $V_{OC}$ down in the 400-500 mV range. Specifically, the last three runs, where the $V_{OC}$’s are in the 500’s, and the $J_{SC}$ values are around 14 mA, closely resemble the best results produced with our early Type I CuGaSe$_2$ devices. However, our best fill factors were less than 60%, which does not agree with the fill factors simulated here, of about 77%. This fact is also reflected in the conversion efficiency numbers, where the simulated numbers of 5-6% are on the higher side of the best efficiencies achieved with our processed sample (slightly less than 5%). This may primarily be because of the extra series resistance that was present in our processed samples, perhaps coming from the presence of multiple (not-so-conductive) phases of the ternary absorber, and defects present in the absorber bulk.

One of the conclusions from our Type I and Type II CuGaSe$_2$ processing experience was that as we successfully raised the $V_{OC}$ (from 500’s to 600’s and rarely 700’s), the $J_{SC}$ values went down from 13-15 mA to about 10-12 mA. For example, for our Type II samples, the typical average $V_{OC}$’s were in high 600’s, whereas the $J_{SC}$’s were in the range of 10-12 mA. To be able to simulate this behavior, we needed to introduce other defect-states into the structure.

The following table includes the parameters used, and the results obtained, for the simulations, where both, interface-defects as well as bulk-defects were introduced in the solar cell structure. Here, the bulk defect states were two acceptor type densities of 2E17 and 1E17, at 0.25 and 0.13 eV from the valence band edge, respectively. These numbers were borrowed from a recent publication where these specific levels were suggested to be present in CuGaSe$_2$ [Zunger].
Table 5.3. SCAPS Simulation Parameters and Results: Bulk- and Interface-States
(Bulk defect states: acceptor/2E17/0.25, and acceptor/1E17/0.13)

<table>
<thead>
<tr>
<th>File name</th>
<th>Interface defects</th>
<th>V&lt;sub&gt;OC&lt;/sub&gt;, Volts</th>
<th>J&lt;sub&gt;SC&lt;/sub&gt;, mA</th>
<th>FF, %</th>
<th>Eff, %</th>
</tr>
</thead>
<tbody>
<tr>
<td>J_p2_1</td>
<td>No defects</td>
<td>1.26</td>
<td>10.81</td>
<td>60.5</td>
<td>8.23</td>
</tr>
<tr>
<td>J_p2i_2</td>
<td>Neutral/ E12/ 0.80</td>
<td>0.521</td>
<td>10.79</td>
<td>73.4</td>
<td>4.12</td>
</tr>
<tr>
<td>J_p2i_3</td>
<td>Donor/ E12/ 0.80</td>
<td>0.433</td>
<td>11.34</td>
<td>74.4</td>
<td>3.65</td>
</tr>
<tr>
<td>J_p2i_4</td>
<td>Acceptor/ E12/ 0.80</td>
<td>0.521</td>
<td>10.79</td>
<td>73.4</td>
<td>4.12</td>
</tr>
<tr>
<td>J_p2i_5</td>
<td>Neutral/ E12/ 0.60</td>
<td>0.520</td>
<td>10.78</td>
<td>73.4</td>
<td>4.11</td>
</tr>
<tr>
<td>J_p2i_6</td>
<td>Donor/ E12/ 0.60</td>
<td>0.363</td>
<td>11.26</td>
<td>60.3</td>
<td>2.46</td>
</tr>
<tr>
<td>J_p2i_7</td>
<td>Acceptor/ E12/ 0.60</td>
<td>0.520</td>
<td>10.78</td>
<td>73.4</td>
<td>4.11</td>
</tr>
<tr>
<td>J_p2i_8</td>
<td>Neutral/ E12/ 0.40</td>
<td>0.520</td>
<td>10.78</td>
<td>73.4</td>
<td>4.11</td>
</tr>
<tr>
<td>J_p2i_9</td>
<td>Donor/ E12/ 0.40</td>
<td>0.369</td>
<td>11.10</td>
<td>65.6</td>
<td>2.68</td>
</tr>
<tr>
<td>J_p2i_10</td>
<td>Acceptor/ E12/ 0.40</td>
<td>0.520</td>
<td>10.78</td>
<td>73.4</td>
<td>4.11</td>
</tr>
<tr>
<td>J_p2i_11</td>
<td>Neutral/ E12/ 0.20</td>
<td>0.532</td>
<td>10.81</td>
<td>75.2</td>
<td>4.32</td>
</tr>
<tr>
<td>J_p2i_12</td>
<td>Donor/ E12/ 0.20</td>
<td>0.509</td>
<td>10.84</td>
<td>77.6</td>
<td>4.28</td>
</tr>
<tr>
<td>J_p2i_13</td>
<td>Acceptor/ E12/ 0.20</td>
<td>0.552</td>
<td>10.45</td>
<td>76.8</td>
<td>4.43</td>
</tr>
<tr>
<td>J_p2i_14</td>
<td>Neutral/ E10/ 0.80</td>
<td>0.670</td>
<td>10.81</td>
<td>77.2</td>
<td>5.60</td>
</tr>
<tr>
<td>J_p2i_15</td>
<td>Donor/ E10/ 0.80</td>
<td>0.669</td>
<td>10.82</td>
<td>77.2</td>
<td>5.58</td>
</tr>
<tr>
<td>J_p2i_16</td>
<td>Acceptor/ E10/ 0.80</td>
<td>0.670</td>
<td>10.81</td>
<td>77.2</td>
<td>5.60</td>
</tr>
<tr>
<td>J_p2i_17</td>
<td>Neutral/ E10/ 0.20</td>
<td>0.675</td>
<td>10.81</td>
<td>77.7</td>
<td>5.66</td>
</tr>
<tr>
<td>J_p2i_18</td>
<td>Donor/ E10/ 0.20</td>
<td>0.673</td>
<td>10.81</td>
<td>77.8</td>
<td>5.66</td>
</tr>
<tr>
<td>J_p2i_19</td>
<td>Acceptor/ E10/ 0.20</td>
<td>0.675</td>
<td>10.80</td>
<td>77.7</td>
<td>5.67</td>
</tr>
</tbody>
</table>

As can be seen from the above table, the first run, where there were two bulk-defects present (but no interface-defects) produced a very high V<sub>OC</sub> of 1.26 V.

However, the J<sub>SC</sub> number, of 10.81 mA, was already in the range of that for the processed devices. When, in addition to the two bulk-defects, some interface-defects were introduced at the density of 1E12, the V<sub>OC</sub> dropped down to the 400’s and 500’s. These
numbers, however, were too low, when compared with the $V_{OC}$’s obtained with our processed samples (most of which are in 600’s and 700’s). Reducing the defect-state-density down to 1E10 brought the $V_{OC}$ back up in high 600’s, while still maintaining the $J_{SC}$ value at around 11 mA. However, once again, the simulated fill factors are somewhat high, and this fact is reflected in the high efficiency of about 5.6%. The following figure depicts the I-V characteristics for some of the simulation runs mentioned above. The high fill factors are quite evident from the significant squared-ness of the curves.

Figure 5.36. I-V Plots for SCAPS Simulation (Bulk and Interface Defects)
The above results closely resemble our processed devices, except for the fill factor values. The low fill factors, obtained for the actual devices, may be a result of a combination of a high series resistance and a low shunt resistance in our samples, which could not be accurately simulated.

Another factor that may affect the $V_{OC}$, and overall performance, of samples is the back contact. We decided to see how the change in the work function of the back contact affected the I-V characteristics. The following figure shows the I-V curves for three values of the back contact work function: 4.53, 4.80 (base value), and 4.65. The absorber layer had the same bulk defects as before: $2E17$ at 0.25 eV, and $1E17$ at 0.13 eV.

![Figure 5.37. I-V Plots for SCAPS Simulation: Back Contact Work Function](image.png)
As is easily evident from the above figure, although the currents seem to be okay, the \( V_{OC} \)'s are still very high. It proved impossible to bring the voltage down substantially, while keeping other parameters in a reasonable range, by varying the back contact work function.

The question about whether CuGaSe\(_2\) forms a true heterojunction has been heavily debated in the recent past. The alternative to a true heterojunction, of course, is a buried homojunction inside the CuGaSe\(_2\) absorber layer. For this to happen, a thin layer near the surface of the absorber would have to be \textit{n-type}, with respect to the deeper, \textit{p-type} bulk of the absorber. Some recent publications, as mentioned in the literature survey, suggest the presence of such an \textit{n-type} layer in CuIn(Ga)Se\(_2\). However, CuGaSe\(_2\) has been suggested to be favoring a true homojunction. We decided to employ the SCAPS technique to see what such an \textit{n-type} top layer, if present, would do to our devices. To accomplish this, a thin (0.1 \( \mu \)m) CuGaSe\(_2\) layer, called CGS2, with 1E14 shallow donors, was introduced on the top of the regular CuGaSe\(_2\) absorber layer. Moreover, we also wanted to see the effect of presence or absence of other layers, such as CdS and ZnO. The following figure shows 7 I-V curves. Each of these curves is associated with a specific set of conditions (as depicted with roman numerals in parentheses beside the curves), and the conditions are described in the text below the figure.
The regular CuGaSe$_2$ layer had two acceptor-type defect-states, with densities $2 \times 10^{17}$ and $1 \times 10^{17}$, at 0.25 eV and 0.13 eV from the valence band edge, respectively (same as the simulations presented before). Other conditions, for the CGS2 layer, as well as other layers in the structure, were:

(i) No CdS or i-ZnO present; CGS2 had 2 defect states, same as the CuGaSe$_2$ layer.

(ii) No CdS or i-ZnO present; No defect-states for CGS2.

(iii) CdS, i-ZnO present; CGS2 had 2 defect-states.
(iv) CdS, i-ZnO present; No defect-states for CGS2.

(v) CdS present; No i-ZnO; No defect-states for CGS2.

(vi) i-ZnO present; No CdS; No defect-states for CGS2.

(vii) CdS, I-ZnO present; 1E12 donors in CGS2.

The most salient feature of the curves is that, whenever there is either CdS or i-ZnO (or both) present, there is a distinct kink that can be seen near the voltage (x) axis. This indicates that, because of the extra n-type CGS2 layer present in the structure, there is an occurrence of some sort of a double-junction in the structure. The only curves that look normal are the ones where there is neither CdS nor i-ZnO present.

Interestingly enough, a few devices from one of our samples had shown the presence of a strong kink near the voltage axis, somewhat like the one seen in the simulated figure. The I-V plot of one of these devices is reproduced below. (It should be noted that the 3-probe I-V plot is oriented differently, compared to the Simulation I-V.)

Figure 5.39. I-V kink in Device # 1 from CuGaSe₂ Sample # P137
However, there was a problem during the ZnO deposition for the above sample. The sample was heated before the actual deposition, but it was realized that the run had to be abandoned because of an issue with the ZnO target. The ZnO deposition was done later, after the issue was resolved. However, the sample had gone through an additional anneal (at about 120°C) for a few hours, in inert atmosphere. The occurrence of a kink such as the one shown above suggests that there may have been a double-junction present in this particular device. This could happen, for example, because of processing problems, such as incorporation of unwanted elements which may have been left behind in the absorber deposition chamber, after, say, CuIn(Ga)Se$_2$ processing. However, the ZnO processing problem suggests that the extended annealing may have hurt the junction, and perhaps, given rise to unwanted diffusion of elements, resulting in the above behavior. However, as mentioned above, such behavior is very rare, and, therefore, seems to suggest that the simulated results don’t really match with our processed devices. It also insinuates that the CuGaSe$_2$ absorber film does not have an n-type surface layer, so the CuGaSe$_2$ devices are the true-heterojunction type devices.

In summary, we had limited success in simulating the behavior of the actual devices, by using SCAPS. The three important conclusions were:

(i) Simultaneous introduction of Interface and Bulk defects in the solar cell structure generated results that were close to the actual device results,

(ii) Changes in the back contact work function could not bring the voltage down to a reasonable value, and

(iii) N-layer simulation experiments indicated the presence of a heterojunction.
5.2.2. AMPS Modeling

AMPS-1D (Analysis of Microelectronic and Photonic Structures: One-Dimensional Approach) was developed by the Pennsylvania State University, in collaboration with the Electric Power Research Institute. The main difference between the SCAPS and AMPS techniques, as it relates to the modeling of our devices, was that SCAPS allowed the incorporation of interface defect-states using a rolled-up parameter called *interface recombination velocity* (somewhat like the *surface recombination velocity* used at the semiconductor and metal surfaces). In a way, this made it easier to experiment with the interface defects, just by changing this velocity number. In AMPS, on the other hand, no such parameter was available. The same effect had to be produced by incorporating defects in the layers that formed the interface, and by manipulating other characteristics such as the affinity and the Bandgap, etc. Another relevant difference between the two techniques was that AMPS used the so-called *back-contact energy*, to specify where the back contact energy bands were, with respect to the bands of the semiconductor (absorber) layer. This value is calculated from the conduction band edge (Ec) of the CuGaSe₂ absorber. In SCAPS, the relevant parameter was the work function of the contact.

In terms of the graphical representation of I-V characteristics, the AMPS plots are inverted, as will be seen shortly. Also, because the AMPS plots show only the one side of the voltage axis, the forward curve can be seen on the same side of the voltage axis, and this results in a negative sign being attached to the fill factor and $V_{OC}$ numbers, with the $J_{SC}$ positive. Similarly, the AMPS energy band diagrams typically show the
equilibrium band diagram at the bottom, and the non-equilibrium diagram at the top of the figure. Once these minor details are understood, it’s easy to study these AMPS plots.

The simulation runs that we carried out are described next. The figures are all together, after the end of this discussion.

Most of the parameters used for the solar cell structure were the same as the ones used for the SCAPS simulations, unless otherwise specified. However, our approach to AMPS was a little different. The CuGaSe$_2$ absorber was created using the main, base layer, along with a thinner (0.1 µm) top layer, so that properties of the bulk and the surface (or near-surface) of the absorber could be controlled rather independently. The thin top layer will sometimes be referred to as the $n$ layer, or $n$-$CuGaSe_2$ layer, although, all this means is that this layer may be similar to, or slightly $n$-type with respect to, the base layer, depending upon the doping levels.

It has been suggested by Zunger, et al. that the increase in the band gap ($E_g$) of CuIn(Ga)Se$_2$ because of increased Ga percentage is due to the conduction band edge ($E_C$) moving up, while the $E_V$ stays the same. We, hence, started out our CuGaSe$_2$ simulations by using the known CuIn(Ga)Se$_2$ parameters, and then lowering the affinity to 3.35, and increasing the band gap to 1.6 eV. The front electrode contact was assumed to be ZnO, the same as that for CuIn(Ga)Se$_2$. The affinity value used for ZnO was 3.7 eV. This first run is labeled as $basecgs$, and Figure 5.40 depicts the two band diagrams for this run.

The bottom diagram is at equilibrium, while the top one is drawn at 1 Volt forward bias. In forward bias, the bands in the CuGaSe$_2$ are beyond the flat-band condition. However, because of the low value of the affinity, the barrier presented by the high $E_C$ is quite high, and prevents electrons from entering. Figure 5.41 shows the light I-V characteristics for
the basecgs run (The solid lines. The dashed curve is discussed next). It can be seen, from the I-V curve, that the efficiency is nearly 18%, with $J_{SC}$ at 18 mA/cm$^2$ and $V_{OC}$ at 1.17 Volts, with an FF of about 80%.

The next task was to lower the $V_{OC}$. It has been claimed that the easily formed defect Cu$_{Ga}$ is at the same location (0.29 eV from $E_V$) as the defect Cu$_{In}$ [Zunger]. Hence, a defect was added to the $n$ and base layers, at 1.31 eV from the $E_C$, at the densities of 1E17 and 1E18, respectively. The dashed I-V curve in Figure 5.41 is the result of this simulation. As can be seen, there is only a small drop in the $V_{OC}$, whereas the $J_{SC}$ and ff are significantly reduced.

Next, acceptor type defects were placed at midgap, but this did not seem to have a strong effect on the characteristics. The large band gap of the absorber material seemed to control the behavior. Therefore, the n layer was doped to the 1E17 level. This would create the junction inside of the absorber material, between the n and base layers, thereby making it a buried homojunction. Figures 5.42 and 5.43 show the resulting band diagram and the I-V behavior, respectively. As can be seen, while the $J_{SC}$, ff and efficiency were all strongly affected, the $V_{OC}$ still remained at over 1 Volt. Moreover, this seemed to distort the I-V curve, with a distinct kink-like behavior, which is not normally observed in the processed samples.

Until this point, it was clear that nothing could bring the $V_{OC}$ down to the level seen in our processed devices, although the other parameters were very much in the range of the processing results. As the primary cause of this was thought to be the height of the $E_C$ above the contact, we decided to increase the affinity value of CuGaSe$_2$ to see if anything changed. The affinity was increased to 3.65 eV. The results are displayed in

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Figure 5.44 (solid lines). As can be easily seen, the I-V curve shape was recovered, but the $V_{OC}$ still stayed high. Next, the acceptor defect density in the n layer was raised to the 1E21 level. As seen in the dashed curve in figure 5.44, this brought the $V_{OC}$ down to 761 mV. However, the $J_{SC}$ dropped to a meager 2.7 mA/cm$^2$, an unreasonably low value. It seemed that, to be able to lower the $V_{OC}$’s, while maintaining the $J_{SC}$ in the range of 10-13 mA/cm$^2$, the affinity would have to be increased further. However, this did not agree with the recent theoretical work in the literature, and, therefore, we decided to try a different approach, as described next.

Figure 5.45 presents the spectral response curves for the above simulation experiments.

Another parameter that has a strong effect on $V_{OC}$ is the back contact. We, therefore, decided to vary the back contact energy in the next few simulation runs. As a reminder, this energy is calculated from the conduction band edge of the bulk CuGaSe$_2$ layer. For the basecgs run, we had used a value of 1.6 eV. This value was now lowered, first to 1.0 eV, and then to 0.8 eV. The results are shown in Figure 5.46. It was found that, once the contact was above the $E_f$, a proportional drop occurred in the $V_{OC}$ value. For the 1.0 eV back contact energy case, the $V_{OC}$ dropped down to 833 mV. Other values were: $J_{SC} = 15.717$ mA/cm$^2$, efficiency = 8.303% and ff = 60%. Although the $J_{SC}$ and ff were around the highest we had seen in our Type I devices (15.2 mA/cm$^2$ and 58%, respectively), the other numbers were still too high. The $V_{OC}$ needed to be around 600-700 mV, and the efficiency around 5%. The back contact energy value of 0.8 eV yielded such results, those being: $V_{OC} = 633$ mV, $J_{SC} = 15.437$ mA/cm$^2$, efficiency = 5.977%, ff = 58.1%. This seemed to be in reasonably good agreement with our (Type I) devices. The
slight discrepancy in the efficiency is a result of the simulated $J_{SC}$ being slightly on the higher side of the $J_{SC}$ value of the processed samples.

The same figure (Figure 5.46) includes a few more curves, obtained by adding some defects in the absorber. It can be easily seen that these defects have essentially distorted the I-V curve shapes, and, hence, cannot be accepted as describing our processed samples. The two cases mentioned above (1.0 eV and 0.8 eV) are the ones that did not have these additional defects, and these yielded normal curve shapes.

There is yet another similarity between the above simulation run and the results of our processed devices. For the processed samples, the I-V curve typically shows an upward slope as the reverse bias increases. This characteristic slope is also observed in the above-mentioned simulated I-V curves. Such a behavior could either be indicative of shunting in the samples, or, more likely, could result from widening of the depletion region, leading to enhanced carrier collection, as the reverse bias increases.

This, then, means that the back contact has a stronger effect on lowering the $V_{OC}$ for the CuGaSe$_2$ devices. (Changes in other parameters, such as defects, can lower the $V_{OC}$ to some extent, but typically result in poor curve shapes.) Indeed, the textbook value (Sze) of 4.8 eV, for the work function of the Molybdenum back contact, would place the contact near the 0.8 eV case mentioned above.

At this point, it was realized that a better fit to our actual data could be obtained if the band gap of CuGaSe$_2$ was increased to 1.65 eV (from the value of 1.6 eV used earlier). This new base simulation run was then labeled as basecgs1.65, and Figures 5.47 and 5.48 depict the band diagram and the I-V characteristics, respectively. The spectral response curves, with and without a forward bias of 1 Volt, are shown in Figure 5.49. As
can be easily seen from comparison of the two curves, there is a loss of current because of poor collection, in the forward bias. Poor transport properties that result into this behavior may be the reason why it is difficult to maintain the $J_{SC}$, while trying to lower the $V_{OC}$ value.

Next, with the new Eg value of 1.65 eV, the back contact energy was progressively lowered, from 1.4 to 1.2, to 1.0, and lastly, to 0.8 eV. Figure 5.50 presents the I-V results for these experiments. Once again, the 0.8 eV case offers the best fit to the results obtained with processed (Type I) samples. The next figure, Figure 5.51, shows the band bending that results from the lowering of the back contact energy.

Because the large band gap of ZnO is the cause of the high $V_{OC}$’s in the preceding simulations, in the next few runs, we decided to leave the ZnO, as well CdS out. The base run with this structure is now labeled as basecg$\text{s1.65nocdsorzn}$o. The I-V characteristics for this run is shown in Figure 5.52, along with those for runs where defect levels were introduced in this structure. It is noteworthy that the efficiency for the base run is as high as 18.769%. It is also interesting to note that high defect levels quickly destroy the $J_{SC}$, just like the case when both CdS and ZnO were present.

Ideally, with the band gap of 1.65, and appropriate doping of the absorber, it is possible to raise the efficiency of a CuGaSe$_2$ structure to above 20%. Figure 5.53 shows the simulated I-V curves for such high-efficiency devices.

In summary, the AMPS simulations that involved variations in the back contact properties yielded a close match with the experimental results. In addition, these simulations also showed that, ideally, an efficiency of above 20% is possible with these solar cells.
It should be mentioned here that, in some of our processing experiments, we did try to change the back contact of the absorber material. The way we tried to do this was not by replacing Molybdenum, but by depositing In, instead of Ga, as the first layer of the absorber material. The hope was that this would modify the actual back contact that the solar cell had. However, the performance of these runs was diminished, and it was attributed to the mixing of In with other elements of the absorber (Cu, Ga, and Se), thereby forming a CuInSe$_2$-CuGaSe$_2$ mix compound. The efforts to change the “back contact”, hence, were unsuccessful.

The next few pages contain figures 5.40-5.51, which relate to the above discussion, after which, the Conclusions of our research are presented.
Figure 5.40. AMPS-1

Basecgs Run:  

\[ Ec \]

1-Volt Forward Bias

\[ Ev \]

Thermodynamic Equilibrium

\[ Ef \]

\[ Ec \]

\[ Ev \]

\[ Ef \]

\[ -9.00E+00 \]  

\[ -8.00E+00 \]  

\[ -7.00E+00 \]  

\[ -6.00E+00 \]  

\[ -5.00E+00 \]  

\[ -4.00E+00 \]  

\[ -3.00E+00 \]  

\[ -2.00E+00 \]  

\[ -1.00E+00 \]  

\[ 0.00E+00 \]  

\[ 1.00E+00 \]  

\[ 2.00E+00 \]  

\[ 3.00E+00 \]  

\[ 4.00E+00 \]  

\[ 5.00E+00 \]  

\[ 6.00E+00 \]  

\[ 7.00E+00 \]  

\[ 8.00E+00 \]  

\[ 9.00E+00 \]  

Position (μm)

Data generated by AMPS-1D, Copyright (c) 1997 The Pennsylvania State University and Electric Power Research Institute
Figure 5.41. AMPS-2
Figure 5.42. AMPS-3
Figure 5.43. AMPS-4
Figure 5.44. AMPS-5
Figure 5.45. AMPS-6
Figure 5.46. AMPS-7
Figure 5.47. AMPS-8
Figure 5.48. AMPS-9

Data generated by AMPS-1D, Copyright (c) 1997 The Pennsylvania State University and Electric Power Research Institute
Figure 5.49. AMPS-10
Figure 5.50. AMPS-11
Basecgs1.65, with 0.8eV back contact energy

Data generated by AMPS-1D, Copyright (c) 1997 The Pennsylvania State University and Electric Power Research Institute

Figure 5.51. AMPS-12
Figure 5.52. AMPS-13
Figure 5.53. AMPS-14

Data generated by AMPS-1D, Copyright (c) 1997 The Pennsylvania State University and Electric Power Research Institute
CHAPTER 6.
CONCLUSION

The accomplishment of this research project was two-fold:

(i) The (modified) manufacturing-friendly, sequential deposition process was used to establish a base CuGaSe$_2$ process, and was then optimized to gain substantial improvements in the performance (especially, the $V_{oc}$) of our CuGaSe$_2$ solar cells,

(ii) The $V_{oc}$ improvement gained in this project is belittled by the high $V_{oc}$ value theoretically predicted for a CuGaSe$_2$ structure. This pointed to a performance ceiling for the material and the process. Therefore, numerous physical, as well as simulation experiments were carried out, which helped improve our understanding of this limitation.

Our EDS results (on a Type II sample) showed that the ratios of the three (Cu, Ga, Se) elements present in the absorber layer were close to 1:1:2, which meant that the material was close to being CuGaSe$_2$, at least in the top region of the film. XRD analysis (also on a Type II sample) showed that the structure of the analyzed CuGaSe$_2$ film was polycrystalline, with a preferred orientation along the [112] direction.

The spectral response curves showed that the bandgap of our CuGaSe$_2$ material was around 1.63 to 1.64 eV. This indicated towards the formation of a material that was very close to the ideal CuGaSe$_2$ absorber material. Also, the response curves showed the presence of a very thin CdS layer, perhaps less than a 100 A$^0$. It is possible that this layer
was not a true CdS layer, but was rather present as an intermediate phase, or mixture, between CdS and the adjoining ZnO top contact layers. This is one area where more systematic experimentation is needed.

The major part of this study entailed the processing of CuGaSe$_2$ solar cells using the Type I and Type II recipes for the absorber formation. There are several differences between the two recipes, in terms of the processing and the results they accomplished. These are listed below, along with the best I-V characteristics obtained for each of the recipes:

(i) In Type I, all of the Ga was deposited up front, before Cu, whereas, for Type II, the Ga was split into two layers, one before, and another after, Cu.

(ii) Typically, a Type II sample saw a higher temperature for a longer period of time. Because this made the substrate more vulnerable to the loss of III-VI species, the process was adjusted so that much more Se was available during a Type II run.

(iii) Variations in the thickness of the initial Ga layer changed the outcome of Type I samples, whereas they had little effect on Type II samples.

(iv) Type II samples had improved $V_{OC}$ values, compared to Type I. The better $V_{OC}$ values for Type II samples were around 725 mV, with the best one at 735 mV. Annealing treatment increased this number to 775 mV. The highest $V_{OC}$ for a Type I sample was 699 mV, with most other “high” values between 650 and 699 mV.

(v) The $J_{SC}$ (current density) performance of Type II samples was diminished, when compared to that of Type I samples. Typical values for Type I were between 13 and 15 mA/cm$^2$, with the best one at 15.2 mA/cm$^2$ (not in the same sample that showed the best $V_{OC}$). Typical values for Type II samples were between 10 and 12 mA/cm$^2$. 

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The above results indicate towards a basic structural difference between the Type I and Type II processing recipes. Such a difference was intended, in that Type II was an attempt towards raising the $V_{OC}$’s by utilizing the Cu-poor-to-Cu-rich film conversion. Although this $V_{OC}$ improvement was accomplished, it was at the cost of the $J_{SC}$, keeping the overall efficiency nearly the same. Repeated efforts to decouple the voltage and current behavior were unsuccessful. Such a decoupling is needed, in order to improve the overall performance.

The shunting effect (as seen in the I-V characteristics) was successfully reduced by optimizing the thickness of the absorber layer. This resulted in a better curve-shape, and improved fill factor values, with the best one at 58%. This also resulted in the best efficiency value of 4.8%.

As mentioned above, annealing, at a high temperature ($200^0$C), improved the $V_{OC}$’s, while somewhat reducing the current performance. Neither annealing at a lower temperature, nor light soaking, showed any specific trend.

Experiments with other layers in the solar cell structure shed some light on the complexity of the material. Efforts to replace CdS, as the heterojunction partner, had very limited success, once again re-establishing CdS as the right choice. These experiments, however, improved our understanding about the CdS process itself. The best CuGaSe$_2$ results have been achieved, elsewhere, by making variations in the CdS process. Although all the details of this work couldn’t be known, a similar effort with our CdS was unsuccessful. Further research is needed, to focus on this aspect.

Efforts were also made to intentionally form an n-type layer at the top surface of the absorber, resulting in little success. This experience, along with the SCAPS
simulation experiments, indicates towards the strong possibility of the junction being a true heterojunction.

The two simulation techniques were helpful in separating the effects of various parameters on the device performance. SCAPS simulation produced a close match to our Type I (processed) devices. This needed the introduction of interface, as well as bulk-defects in the solar cell structure. AMPS simulation, on the other hand, placed the blame on the back contact. (SCAPS produced no such results when the back contact properties were changed.)

Because of the unavailability of an alternate back contact material (and process) in our laboratory, actual (physical) experimentation with the back contact could not be carried out. Such experimentation is needed, to make use of the simulated results, and to better understand the source of the limitation on the $V_{OC}$ of the CuGaSe$_2$/CdS solar cell structure.
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APPENDICES
APPENDIX A. EDS and XRD Results

The EDS are XRD results for a CuGaSe$_2$ Type II sample are presented below.

EDS Results for Sample # P131
XRD Results for Sample # P131
ABOUT THE AUTHOR

Although born and brought up in India, Mr. Panse has a strong disbelief in
*Arranged Marriages.* He is married to his childhood friend Pradnya. Moreover, Mr.
Panse is a *confirmed (Russelian) agnostic,* and *Reason* (along with *Murphy’s Laws,* and
the wife) is his guiding principle in life. He also holds highest the virtues of peace,
freedom, democracy, and non-violence.

Mr. Panse grew up in the city of Thane, in Western India. He obtained his
Bachelor’s in Physics from the University of Bombay (now Mumbai). Later, he came to
the United States, to attend the University of South Florida, for his graduate study in
Physics. He, then, went on to obtain his Ph.D. in Electrical Engineering.

In addition to using it for his family’s well-being, Mr. Panse plans to use his
knowledge and experience for the betterment of the community. Right now, he is not
sure how. But he will figure it out, eventually!