LOW-POWER SOFTWARE CONFIGURABLE MODULATOR FOR WIRELESS COMMUNICATIONS

By

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by

Xiuge Yang
To my parents.
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# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>ACKNOWLEDGMENTS</th>
<th>iv</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIST OF TABLES</td>
<td>vii</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>viii</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td>xiv</td>
</tr>
<tr>
<td>CHAPTER</td>
<td></td>
</tr>
<tr>
<td>1 INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>1.1 Software Defined Radio</td>
<td>1</td>
</tr>
<tr>
<td>1.2 Digital Modulation Schemes</td>
<td>3</td>
</tr>
<tr>
<td>1.2.1 Binary Phase Shift Keying</td>
<td>4</td>
</tr>
<tr>
<td>1.2.2 Quadrature Phase Shift Keying</td>
<td>5</td>
</tr>
<tr>
<td>1.2.3 Offset Quadrature Phase Shift Keying</td>
<td>7</td>
</tr>
<tr>
<td>1.2.4 Minimum Shift Keying</td>
<td>8</td>
</tr>
<tr>
<td>1.2.5 Gaussian Minimum Shift Keying</td>
<td>9</td>
</tr>
<tr>
<td>1.2.6 Amplitude Modulation</td>
<td>10</td>
</tr>
<tr>
<td>1.3 Overview of Dissertation</td>
<td>12</td>
</tr>
<tr>
<td>2 SOFTWARE CONFIGURABLE MODULATOR</td>
<td>14</td>
</tr>
<tr>
<td>2.1 Conventional I/Q Modulators</td>
<td>14</td>
</tr>
<tr>
<td>2.2 Proposed Software Configurable Modulator</td>
<td>16</td>
</tr>
<tr>
<td>2.3 Comparison between Conventional and Proposed Modulators</td>
<td>20</td>
</tr>
<tr>
<td>3 DESIGN OF A TEST MODULATOR FOR FIXED PATTERNED DATA</td>
<td>22</td>
</tr>
<tr>
<td>3.1 Constant Envelope Modulation</td>
<td>22</td>
</tr>
<tr>
<td>3.1.1 Phase Change Pattern for MSK modulation</td>
<td>23</td>
</tr>
<tr>
<td>3.1.2 Phase Change Pattern for GMSK Modulation</td>
<td>24</td>
</tr>
<tr>
<td>3.1.3 Designed Constant Envelope Phase Shift Test Modulator</td>
<td>28</td>
</tr>
<tr>
<td>3.2 Design Issues Associated With the Constant Envelope Phase Shift Modulator</td>
<td>29</td>
</tr>
<tr>
<td>3.2.1 Theoretical Power Spectral Density with respect to the Number of Phase Shifts per Bit Period</td>
<td>29</td>
</tr>
<tr>
<td>3.2.2 Impact of Variations in the Modulated Signal’s Amplitude and Phase Shift Step</td>
<td>31</td>
</tr>
</tbody>
</table>
### 3.3 Circuit Description
- 3.3.1 Divider ........................................... 35
- 3.3.2 Multiplexers ...................................... 37
- 3.3.3 Phasor Combining Circuit ...................... 39
- 3.3.4 Buffers ............................................ 40
- 3.3.5 Digital Circuit Section ......................... 41

### 3.4 Experimental Results
- 3.4.1 Modulator IC Fabricated in 0.18 µm CMOS Process ...... 42
- 3.4.2 Modulator IC Fabricated in 0.13 µm CMOS Process ...... 50
- 3.4.3 Performance Comparison ............................ 54

### 4 A DIGITALLY CONTROLLED PHASE SHIFT MODULATOR FOR ARBITRARY DATA PATTERNS ............................................. 57
- 4.1 Design Details ....................................... 57
- 4.2 Experimental Results ................................. 61

### 5 DESIGN OF A DIRECT CONVERSION TRANSMITTER ............. 73
- 5.1 Direct Conversion Transmitters .............. 73
- 5.2 Design of an Inductor-Capacitor-Based Voltage Controlled Oscillator 75
  - 5.2.1 Small Signal Model of a CMOS VCO ........... 77
  - 5.2.2 Noise Issue Considerations .................. 79
- 5.3 Design of a Power Amplifier .................. 82
  - 5.3.1 Basic Characteristics of a Power Amplifier .. 82
  - 5.3.2 Classes of Power Amplifiers ................. 84
  - 5.3.3 Design of a Nonlinear Power Amplifier for the Output of the Constant Envelope Modulator Circuit .................. 88
- 5.4 Experimental Result of the Direct Conversion Transmitter Circuit 92
- 5.5 Direct Conversion Transmitter using a Quadrature Voltage Controlled Oscillator .............................................. 100
  - 5.5.1 Design of a Quadrature Voltage Controlled Oscillator 101
  - 5.5.2 Experimental Result of the Transmitter Circuit using QVCO 106

### 6 DESIGN OF An OQPSK MODULATOR .......................... 110
- 6.1 Design of the Modulator Circuit Board ............. 110
- 6.2 Experimental Results .................................. 117

### 7 SUMMARY AND FUTURE WORK .............................. 126
- 7.1 Summary ............................................. 126
- 7.2 Future Work .......................................... 130

### REFERENCES .............................................. 134

### BIOGRAPHICAL SKETCH ..................................... 138
### LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3–1</td>
<td>Summary of the phase change pattern of GMSK modulation</td>
</tr>
<tr>
<td>3–2</td>
<td>Summing weights for generating different phasors</td>
</tr>
<tr>
<td>3–3</td>
<td>Summary of modulator performance (0.18 µm chip)</td>
</tr>
<tr>
<td>3–4</td>
<td>Summary of modulator performance (0.13 µm chip)</td>
</tr>
<tr>
<td>3–5</td>
<td>Comparison of modulator performance</td>
</tr>
<tr>
<td>4–1</td>
<td>Performance summary of the modulator for arbitrary data patterns</td>
</tr>
<tr>
<td>5–1</td>
<td>Performance summary of the direct conversion transmitter</td>
</tr>
<tr>
<td>5–2</td>
<td>Performance summary of the direct conversion transmitter using a QVCO</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1–1</td>
<td>The QPSK modulation. The input bit stream is separated into two streams containing odd and even bits.</td>
</tr>
<tr>
<td>1–2</td>
<td>A QPSK signal waveform</td>
</tr>
<tr>
<td>1–3</td>
<td>OQPSK is obtained from QPSK by delaying the odd bit stream by half a bit interval with respect to the even bit stream</td>
</tr>
<tr>
<td>1–4</td>
<td>An OQPSK signal waveform</td>
</tr>
<tr>
<td>1–5</td>
<td>Power Spectral Density of an MSK signal as compared to a QPSK or OQPSK signal</td>
</tr>
<tr>
<td>1–6</td>
<td>Constellation of a GMSK signal. An MSK signal has a similar constellation in that the amplitude (envelope) does not vary.</td>
</tr>
<tr>
<td>1–7</td>
<td>Power Spectral Density of a GMSK signal at different BT product</td>
</tr>
<tr>
<td>1–8</td>
<td>Constellation of a 16-QAM signal</td>
</tr>
<tr>
<td>2–1</td>
<td>Block diagram of a generic I/Q modulator</td>
</tr>
<tr>
<td>2–2</td>
<td>Phasor diagram of a modulated signal</td>
</tr>
<tr>
<td>2–3</td>
<td>How a phasor can be generated from two phasors in quadrature</td>
</tr>
<tr>
<td>2–4</td>
<td>Conceptual schematic of a summing circuit</td>
</tr>
<tr>
<td>3–1</td>
<td>An MSK modulation example and the modulated signal’s constellation (a) MSK modulation is I-Q modulation with half sinusoidal pulse shaping (b) The modulated signal presents a constant envelope constellation</td>
</tr>
<tr>
<td>3–2</td>
<td>ADS simulation for GSM</td>
</tr>
<tr>
<td>3–3</td>
<td>ADS simulated GMSK waveform (a) I-channel (b) Q-channel</td>
</tr>
<tr>
<td>3–4</td>
<td>ADS simulation for GMSK spectrum</td>
</tr>
<tr>
<td>3–5</td>
<td>MATLAB simulation of the constellation of a GMSK signal</td>
</tr>
<tr>
<td>3–6</td>
<td>Boundary points for one bit interval on a GMSK constellation</td>
</tr>
</tbody>
</table>
3–7 Comparison of power spectral density (PSD) with respect to the number of phase shifts per bit period. Normalized frequency is used in the figure.

3–8 Ideal constellation of the modulator output.

3–9 Normalized sidelobe level (referenced to mainlobe level) versus variations in amplitude and phase shift (The X-axis has a unit of radians for phase shift variation, and it indicates percentage for amplitude variation).

3–10 How four discrete phasors within a quadrant can be generated from two phasors in quadrature.

3–11 Constant envelope phase shift modulator.

3–12 A 2:1 static frequency divider (a) Block diagram (b) A detailed divider schematic.

3–13 A 2:1 differential current-steering multiplexer.

3–14 Phasor combining circuit.

3–15 Schematic of the buffer.

3–16 Flip-flop latch.

3–17 Die microphotograph of the modulator IC (0.18 µm chip).

3–18 Simulated output power spectrum for the fixed repetitive data pattern.

3–19 Measured output power spectrum. Signal’s frequency is 25 MHz, or one fourth of the 100 MHz bit rate, lower than the 2.5 GHz carrier frequency.

3–20 Measured constellation (0.18 µm chip) of the modulated signal (EVM = 2.8%). The signal moved sequentially and repetitively in full circles.

3–21 Measured I/Q plane diagram (0.18 µm chip) of the modulated signal.

3–22 Measured EVM vs. carrier frequency (0.18 µm chip). At 100 Mbps bit rate, for EVMs lower than 5.5%, the modulator can operate at a carrier frequency between 1.75 GHz and 3.5 GHz.

3–23 Measured EVM vs. bit rate (0.18 µm chip). At 2.5 GHz carrier frequency, for EVMs lower than 5%, the bit rate of the modulator ranges from DC to 500 Mbps.

3–24 Constellation (EVM = 6%) at bit rate greater than 500 Mbps (0.18 µm chip).

3–25 When the error vector is perpendicular to the ideal phasor, the phase variation is the biggest.
3–26 When the error vector is in the same direction as the ideal phasor, the amplitude variation is the biggest.

3–27 Complete modulator test chip circuit (0.13 µm chip).

3–28 Die microphotograph of the modulator IC (0.13 µm chip).

3–29 Measured constellation (0.13 µm chip) of the modulated signal (EVM = 3.5%).

3–30 Measured I/Q plane diagram (0.13 µm chip) of the modulated signal.

3–31 Measured EVM vs. carrier frequency (0.13 µm chip). At 100 Mbps bit rate, for EVMs lower than 4%, the modulator can operate at a carrier frequency between 1.5 GHz and 3.3 GHz.

3–32 Measured EVM vs. bit rate (0.13 µm chip). At 2.5 GHz carrier frequency, for EVMs lower than 5.5%, the bit rate of the modulator ranges from DC to 225 Mbps.

4–1 Movement of the phasor when serial data stream 10110010 is MSK modulated.

4–2 Boundary phases on the constellation for the 8 bit intervals.

4–3 How a state stream can be generated at the output of a MUX.

4–4 Modulator circuit for arbitrary data patterns.

4–5 Ideal normalized output PSD for the modified modulator if pseudo random input data are applied.

4–6 Ideal constellation for the modified modulator if pseudo random input data are applied.

4–7 Die microphotograph of the modulator circuit for arbitrary data patterns.

4–8 Measurement setup for testing the modulator circuit with pseudo random input data bits.

4–9 Measured constellation at 2.5 GHz carrier frequency and 12 Mbps bit rate.

4–10 Measured I/Q diagram at 2.5 GHz carrier frequency and 12 Mbps bit rate.

4–11 Measured power spectrum at 2.5 GHz carrier frequency and 12 Mbps bit rate.

4–12 Measured power spectrum with a smaller frequency span at 2.5 GHz carrier frequency and 12 Mbps bit rate.
4–13 Simulated power spectrum of the modulator output with pseudo random input data bits ............................................. 68
4–14 Measured power spectrum at 2.5 GHz carrier frequency and 50 Mbps bit rate .......................................................... 69
4–15 Measured power spectrum at 2.5 GHz carrier frequency and 100 Mbps bit rate .......................................................... 69
4–16 IEEE 802.15.4 and ZigBee working model ......................................................... 70
4–17 Output spectrum of the CC2420 transmitter ......................................................... 71
5–1 Generic direct conversion transmitter utilizing the conventional I/Q modulator .......................................................... 74
5–2 Designed direct conversion transmitter to be designed utilizing the constant envelope phase modulator ......................... 76
5–3 Designed CMOS LC-VCO ........................................................................... 77
5–4 Equivalent circuit model of the designed CMOS LC-VCO ..................................... 78
5–5 Symmetric spiral inductor model ...................................................................... 79
5–6 Layout of the LC-VCO circuit .......................................................................... 81
5–7 Simulated result of the output of VCO plus divider ............................................... 83
5–8 Voltage-current relationships for various classes of PA ........................................ 85
5–9 Topology of a single-ended power amplifier (class A, B, and C) .......................... 88
5–10 Buffers to drive the PA. (a) Buffer for the first three stages (b) Buffer for the last stage ................................................................ 89
5–11 Layout of the PA and its proceeding buffer/driver ............................................... 90
5–12 Simulated differential output waveform from the PA ........................................ 91
5–13 Die microphotograph of the direct conversion transmitter circuit .................... 93
5–14 Measurement setup for testing the transmitter circuit ........................................ 94
5–15 Observed output signals through substrate coupling from the LC-VCO at 5 GHz and the divider of the modulator at 2.5 GHz ................................................................. 95
5–16 Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 12 Mbps bit rate ................................................................. 96
5–17 Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 25 Mbps bit rate ................................................................. 97
5–18 Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 37.5 Mbps bit rate ................................. 97
5–19 Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 50 Mbps bit rate ................................. 98
5–20 Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 100 Mbps bit rate ................................. 98
5–21 Output RF power level of the transmitter circuit vs. carrier frequency ................................. 99
5–22 Direct conversion transmitter to be designed ................................. 101
5–23 Quadrature VCO ......................................................................... 102
5–24 Designed LC-QVCO ..................................................................... 102
5–25 Layout of the LC-QVCO .................................................................. 103
5–26 Simulated result of the quadrature LO signals generated by the QVCO ........................................................................... 105
5–27 Block diagram of the direct conversion transmitter utilizing an LC-QVCO ....................................................... 105
5–28 Die microphotograph of the direct conversion transmitter circuit ....................................................... 106
5–29 Measured power spectrum of the transmitter circuit using a QVCO at 2.56 GHz carrier frequency and 12 Mbps bit rate ....................................................... 108
5–30 Measured power spectrum of the transmitter circuit using a QVCO at 2.56 GHz carrier frequency and 25 Mbps bit rate ....................................................... 108
5–31 Measured power spectrum of the transmitter circuit using a QVCO at 2.56 GHz carrier frequency and 37.5 Mbps bit rate ....................................................... 109
6–1 Phasor combining approach ................................................................. 111
6–2 Implementation of software control for MSK modulation ................................................................. 112
6–3 Constellation of an OQPSK signal ........................................................ 112
6–4 Illustration of how the correct quadrants can be selected by the multiplexers for OQPSK ................................................................. 113
6–5 Modulator core circuit ................................................................. 114
6–6 Die microphotograph of the modulator core circuit ................................................................. 115
6–7 Using Linecalc to calculate the width of microstrip transmission line on an FR4 board ................................................................. 116
6–8 Layout of the printed circuit board designed in Protel ................................................................. 117
6–9 Bonding diagram for the core circuit chip ........................................ 118
6–10 Photo of the bonded chip on the PC board ........................................ 118
6–11 Photo of the completed PC board ...................................................... 118
6–12 Measurement setup for testing the modulator board .......................... 119
6–13 Schematic of the board-level current source ........................................ 119
6–14 Photo of the current source test board for OQPSK modulation .......... 119
6–15 Theoretical power spectrum of OQPSK .............................................. 121
6–16 Consistent measurement result with theoretical spectrum .................. 121
6–17 Measured output spectrum at 0.5 GHz carrier frequency and 24 Mbps data rate .................................................. 122
6–18 Measured output spectrum at 3 GHz carrier frequency and 24 Mbps data rate .................................................. 122
6–19 Measured output spectrum at 3.7 GHz carrier frequency and 24 Mbps data rate .................................................. 123
6–20 Measured output spectrum at 2.4 GHz carrier frequency and 40 Mbps data rate .................................................. 123
6–21 Measured output spectrum at 2.4 GHz carrier frequency and 80 Mbps data rate .................................................. 123
6–22 Measured output spectrum at 2.4 GHz carrier frequency and 100 Mbps data rate .................................................. 124
6–23 Comparison of the power spectra for different number of phasors per quadrant .................................................. 124
7–1 Simplified µNode RF subsystem block diagram ................................... 129
7–2 Measured output power spectrum (100 Mbps data rate) and constellation (12 Mbps data rate) around 24 GHz ......................... 129
7–3 How the correct values of I1 and I2 can be provided for a phasor .......... 132
7–4 Die photo of the modulator core circuit using UMC 90 nm technology .. 133
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LOW-POWER SOFTWARE CONFIGURABLE MODULATOR FOR WIRELESS COMMUNICATIONS

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We examined a software configurable modulator with the potential to generate different modulation schemes. The modulator uses a “digital” approach unlike the “mixing” or “multiplying” approach used by conventional analog modulators. The digital approach uses the phasor combining technique to generate the modulated signal constellation. The phasor combing method is essentially to weigh and sum up two phasors, or two LO signals with different phases (e.g., in quadrature) to generate a desired phasor that represents the modulated signal on the constellation.

We designed and tested 2 test modulator circuits realizing an MSK-like modulation scheme based on the design approach: one with a fixed data pattern and the other for arbitrary data patterns. Experimental results showed that, compared to a conventional modulator with similar functions, the proposed modulator has the advantages of low power consumption (∼3.6 mW excluding output buffers), high data rate (up to ∼100 Mbps), broad operating frequency
range (up to \(\sim 3\) GHz), and less circuit complexity in terms of necessary accompanying
circuit components for function and performance purposes.

We also present the design and experimental results of a direct conversion
transmitter that uses the modulator. The transmitter consists of a voltage
controlled oscillator (VCO), the modulator circuit for arbitrary bit patterns,
and a power amplifier (PA). The power consumption of the whole transmitter is
\(\sim 129\) mW, and the output power level is \(\sim 3\) dBm. The transmitter can be used for
a ZigBee-ready personal area network, or other similar wireless networks. It has the
advantages of higher data rate and lower error vector magnitude (EVM) than the
normal specifications for such networks.

We also designed and built a board-level modulator a core modulator chip
with the same architecture as the integrated modulator circuit. Control signals and
bias currents can be applied off-chip by on-board circuit components. The board
was tested for offset quadrature phase shift keying (OQPSK) modulation, and
the minimum shift keying (MSK) function can be developed by properly designed
on-board circuitry.

The phasor combining approach can potentially allow a modulator to generate
different modulation schemes such as QPSK, MSK, and even quadrature amplitude
modulation (QAM). These modulation schemes are widely used in today’s wireless
communications. Therefore, the proposed modulator may be well suited for a
software defined radio.
CHAPTER 1
INTRODUCTION

1.1 Software Defined Radio

The concept of software defined radio is gaining more attention and acceptance, thanks to the third-generation standards. The third-generation standards support adaptive modulation and coding, user (or network) controlled quality of service (QoS), and cooperative networking have necessitated the use of software radio architectures for radio design [1]. This makes it possible for the radio to provide more services by sharing resources with neighboring devices and networks. A multimode handset has the potential for more services and global roaming capability.

Software defined radio (SDR) forum [www.sdrforum.org] defines SDR technology as “radios that provide software control of a variety of modulation techniques, wide-band or narrow-band operation, communications security functions (such as hopping), and waveform requirements of currents and evolving standards over a broad frequency range.” Also known as software radio (SR), it can be seen as wireless communication in which the transmitter modulation is generated or defined by a computer, and the receiver uses a computer to recover the signal. SDR is a rapidly evolving technology generating more and more interest in the telecommunication industry. Many analog radio systems are being replaced by digital radio systems for various radio applications. Programmable
hardware modules are increasingly being used in digital radio systems at different functional levels. SDR technology facilitates implementation of some of the functional modules in a radio system such as modulation/demodulation, signal generation, coding, and link-layer protocols in software. This helps in building reconfigurable software radio systems where dynamic selection of parameters for each of the modules is possible [2]. Therefore, SDR technology greatly broadens the application prospects of a system by allowing the same system to be compatible for applications that use different link-layer protocols and/or modulation/demodulation techniques.

SDR technology aims to implement radio functionality as software modules running on a generic hardware platform. Multiple software modules implementing different standards can be present in the radio system. In other words, SDR is a collection of hardware and software technologies that enable reconfigurable system architectures for wireless networks and user terminals. Therefore, radios built using SDR technology can allow

- Standard, open, and flexible architectures for a wide range of communications products
- Enhanced wireless roaming for consumers by extending the capabilities of current and emerging commercial air-interface standards
- Over-the-air downloads of new features and services as well as software patches
- Advanced networking capabilities to allow truly portable networks
- Unified communication across commercial, civil, federal, and military organizations
- Significant life-cycle cost reductions
To date, software radio base stations have been more popular and gotten more attention than handsets, because base stations have much more relaxed requirements for specifications like power and silicon area. However, software radio designs are migrating to small handsets that support multimode radios, although the task remains challenging due to the many constraints.

1.2 Digital Modulation Schemes

Take as an example a voice SDR transmitter that might be used in a mobile two-way radio or cellular telephone communications. Typically it consists of a microphone, an audio amplifier, an analog-to-digital converter (ADC) that converts the voice audio to ASCII data, a modulator that impresses the ASCII data onto a radio-frequency (RF) carrier, a series of amplifiers that boosts the RF carrier to the power level necessary for transmission, and a transmission antenna. Among these modules, the ADC and the modulator are computer-controllable circuits whose parameters are determined by computer programming (software). The service type, the mode, and/or the modulation protocol can be changed by selecting and launching the requisite computer program.

The modulator is a key component for software configurability of an SDR. Therefore, it is necessary to look at some of the basic digital modulation techniques for wireless communications.

What is digital modulation? To transport data in a digital communication system, typically one or more physical characteristics of a sinusoidal carrier (such
as frequency, phase, or amplitude) is adjusted. A modulator at the transmitter end imposes the physical change on the carrier.

The choice of digital modulation scheme will significantly affect the characteristics, performance, and resulting physical realization of a communication system. Depending on the physical characteristics of the channel and required levels of performance, some modulation schemes will have advantages over others. Other factors that can affect the choice include required data rate, available bandwidth, anticipated link budget, hardware cost and current consumption. Now let us look at some commonly used digital modulation schemes in various wireless communications standards.

1.2.1 Binary Phase Shift Keying

Binary phase shift keying (BPSK) is the simplest form of digital phase modulation. With theoretical BPSK, the carrier phase has only two states. For example, $S_0(t) = A \cos \omega t$ represents binary “0”, and $S_1(t) = A \cos(\omega t + \pi)$ represents binary “1”.

For M-ary phase shift keying (PSK), M different phases are required, and every $n$ (where $M = 2^n$) bits of the binary bit stream are coded as one signal that is transmitted as $A \cos(\omega t + \theta_j)$, where $j = 1, ..., M$. When improved spectral efficiency is required, higher-order modulation schemes, such as quadrature phase shift keying (QPSK), are often used in preference to BPSK.
1.2.2 Quadrature Phase Shift Keying

If we define four signals, each with a phase shift differing by $\pi/2$, then we have quadrature phase shift keying (QPSK). Figure 1–1 shows that, the input binary bit stream, $d_k$ where $k = 0, 1, 2, ..., \text{arrives at the modulator input at a rate } 1/T \text{ bits/sec and is separated into two data streams } d_I(t) \text{ and } d_Q(t) \text{ containing odd and even bits respectively, i.e.,}$

$$d_I(t) = d_0, d_2, d_4, ...$$

$$d_Q(t) = d_1, d_3, d_5, ...$$
A convenient orthogonal realization of a QPSK waveform, \( s(t) \), is achieved by amplitude modulating the in-phase and quadrature data streams onto the cosine and sine functions of a carrier wave as

\[
S(t) \propto d_I(t) \cos \omega t + d_Q(t) \sin \omega t
\]  

Using trigonometric identities this can also be written as

\[
S(t) = A \cos(\omega t + \pi/4 + \theta)
\]

The pulse stream \( d_I(t) \) modulates the cosine function with an amplitude of \( \pm 1 \). This is equivalent to shifting the phase of the cosine function by 0 or \( \pi \). Consequently this produces a BPSK waveform. Similarly the pulse stream \( d_Q(t) \) modulates the sine function, yielding a BPSK waveform orthogonal to the cosine function. The summation of these two orthogonal waveforms is the QPSK waveform. The values of \( \theta(t) \) (0, \(-\pi/2\), \(\pi\), \(\pi/2\)) represent the four possible combinations of \( d_I(t) \) and \( d_Q(t) \). Each of the four possible phases of carriers represents two bits of data. Thus there are two bits per symbol. Since the symbol rate for QPSK is half the bit rate, twice as much data can be carried in the same amount of channel bandwidth as compared to BPSK. This is possible because the two signals I and Q are orthogonal to each other and can be transmitted without interfering with each other.

In QPSK, the carrier phase can change only once every \( 2T \) seconds. If from one \( T \) interval to the next one, neither bit stream changes sign, the carrier phase remains unchanged. If one component \( d_I(t) \) or \( d_Q(t) \) changes sign, a phase change
of 90° occurs. However, if both components change sign, then a phase shift of
occurs (Figure 1–2). In fact, the 180° shift in phase will cause the envelope to go
to zero momentarily. The potential for a 180° phase shift in QPSK results in more
likely spectral regrowth and requires better linearity in the power amplifier.

1.2.3 Offset Quadrature Phase Shift Keying

If the two bit streams $d_I(t)$ and $d_Q(t)$ are offset by a $\frac{1}{2}$ bit interval (Figure
1–3), then the amplitude fluctuations are minimized since the phase never changes
by 180°. This modulation scheme, offset quadrature phase shift keying (OQPSK),
is obtained from QPSK by delaying the odd bit stream by half a bit interval
with respect to the even bit stream. Figure 1–4 shows that, the range of phase
transitions is 0° and 90° (the possibility of a phase shift of 180° is eliminated) and
occurs twice as often, but with half the intensity of the QPSK. The phase of the
carrier is potentially modulated every bit, not every other bit as for QPSK. Hence,
the phase trajectory never approaches the origin. While amplitude fluctuations may
still occur in the transmitter and receiver, they have smaller magnitude. The bit
error rate for QPSK and OQPSK is the same as for BPSK.
Figure 1–3. OQPSK is obtained from QPSK by delaying the odd bit stream by half a bit interval with respect to the even bit stream.

Figure 1–4. An OQPSK signal waveform.

It should be noted that, although OQPSK is obtained from QPSK by delaying $d_Q(t)$ by 1 bit or $T$ seconds with respect to $d_I(t)$, this delay has no effect on the bit error rate or bandwidth. In fact, because of the similarities between QPSK and OQPSK, similar signal spectra and bit error rate are achieved. OQPSK is used in the North America IS-95 CDMA cellular system for the link from the mobile to the base station.

1.2.4 Minimum Shift Keying

Minimum shift keying (MSK) is derived from OQPSK by replacing the rectangular pulse in amplitude with a half-cycle sinusoidal pulse. This sinusoid
Figure 1–5. Power Spectral Density of an MSK signal as compared to a QPSK or OQPSK signal

provides the required linear advancement or receding of phase that makes MSK a continuous phase modulation. The MSK modulation makes the phase change linear and limited to $\frac{\pi}{2}$ over a bit interval $T$. This enables MSK to provide a significant improvement over QPSK. Because of the effect of the linear phase change, the power spectral density (PSD) has low sidelobes that help to control adjacent-channel interference. However the mainlobe becomes wider than the quadrature shift keying. Figure 1–5 [3] shows the PSD comparison between MSK and QPSK/OQPSK.

1.2.5 Gaussian Minimum Shift Keying

In MSK the rectangular pulse is replaced with a sinusoidal pulse. Other pulse shapes are also possible. A Gaussian-shaped impulse response filter generates a signal with low sidelobes and narrower mainlobe than the rectangular pulse. The filter is approximated by a delayed and shaped impulse response that has a Gaussian-like shape. This modulation is called Gaussian minimum shift keying.
(GMSK). Therefore, GMSK is a simple binary modulation scheme which may be viewed as a derivative of MSK. Both modulation schemes are constant-envelope modulations as can be seen from Figure 1–6. But in practice, GMSK is more attractive for its excellent bandwidth efficiency, although inter symbol interference (ISI) is introduced because a Gaussian pulse extends into adjacent bits. The relationship between the premodulation filter bandwidth, $B$, and the bit period, $T$, or the product of the two, determines the bandwidth of the GMSK signal, which is shown in Figure 1–7 [4].

Both MSK and GMSK have constant amplitude waveforms, which allows the power amplifier to be operated further into saturation yielding improved efficiency and increased output power, without significant spectral re-growth. As a variation of MSK, GMSK provides better spectral roll-off in exchange for error rate. The improved roll-off is to comply with demanding wireless standards for adjacent channel interference.

1.2.6 Amplitude Modulation

All the modulation schemes mentioned above are constant envelope modulations. Constant envelope modulations have the following advantages [5].
- Power efficient nonlinear amplifiers can be used without introducing degradation in the spectrum occupancy of the transmitted signal.

- Low out-of-band radiation can be achieved.

- Limiter-discriminator detection can be used, which simplified receiver design and provides high immunity against random FM noise and signal fluctuations due to Rayleigh fading.

However, amplitude modulations are also a very important class of modulation scheme and still find their many applications in wireless communications. One of the most commonly used amplitude modulations is quadrature amplitude modulation (QAM).

QAM actually is a method of combining two amplitude-modulated signals into a single channel, thereby doubling the effective bandwidth. Essentially, it is a combination of amplitude modulation and phase shift keying. In QAM, data
information is encoded into two carrier waves, whose phases are in quadrature, by variation of the carrier amplitude, in accordance with two input signals. As an example, Figure 1–8 shows the constellation of a 16-QAM signal. QAM and its derivatives are used in both mobile radio and satellite communication systems.

1.3 Overview of Dissertation

A software configurable modulator that has the potential to generate different modulation schemes is proposed. The modulator uses a “digital” approach rather than conventional analog modulators using “mixing” or “multiplying” approaches. The digital approach uses the phasor combining technique to generate the modulated signal constellation. The details of the phasor compering method will be explained in Chapter 2. A test modulator with fixed data pattern based on the design approach was built and tested, and is presented in Chapter 3. A modulator for arbitrary data patterns based on the testing results of the test modulator is introduced in Chapter 4. Chapter 5 presents a design and experimental results of a
direct conversion transmitter which integrates a VCO, the modulator circuit, and a PA, demonstrating one of the many possible applications of the modulator. A board-level modulator designed and tested for OQPSK modulation is introduced in Chapter 6. The modulator circuit board has the ability to generate MSK as well. Chapter 7 summarizes the dissertation and talks about future work.
CHAPTER 2
SOFTWARE CONFIGURABLE MODULATOR

2.1 Conventional I/Q Modulators

From the introduction to the different modulation schemes in the previous chapter, it can be seen that, in quadrature schemes, two independent signals (“in-phase” and “quadrature”) are transmitted via a single carrier, making use of the orthogonality of signal components. Cellular standards, such as the international GSM standard, the US IS54, IS95, and IS136 standards, and the Japanese PHS, all require I/Q demodulation in some form. Generally speaking, quadrature phase modulation can be regarded as a special case of quadrature amplitude modulation, where the amplitude of the modulated signal is constant, with only the phase varying. For example, QAM and QPSK systems abound, in the sense that QPSK can be viewed as a 4-QAM modulation. Applications for QAM or QPSK include CATV set-top-box converters and hybrid fiber/coax video transmission.

Modulators are a fundamental component in integrated circuits for wireless communication systems. The most commonly used modulators are I/Q modulators, which operate by taking two baseband data sequences (I and Q channels) and varying the amplitude and phase of a sinusoidal carrier signal in response to the instantaneous I and Q channel voltages [6]. The conceptual block diagram of a generic I/Q modulator is shown in Figure 2–1 [7]. Many modulators designed based on the I/Q quadrature scheme have been reported such as in [8], [9], and [10].
The modulation schemes introduced in the last chapter are all quadrature modulations (except for BPSK). Choice of modulation scheme is a tradeoff between the transmit spectrum, simplicity of detection, and error rate performance. If we consider QPSK as a variety of QAM, or 4-QAM, then these modulations can be divided into two categories: linear and constant envelope. Linear modulations such as QAM require linear amplification because the data information is carried in the signal’s amplitude variations, whereas constant envelope modulations such as GMSK are more robust to the distortion caused by nonlinear amplifiers, which offer higher power efficiency. There is no one prominent modulation scheme between linear and constant envelope modulation methods, because when it comes to particular application, it is important to look at the tradeoffs involved. For example, QPSK’s importance in CDMA is evident with its efficient bandwidth use, enabling more users within a limited channel bandwidth. GMSK makes its contribution to cellular systems in communications that necessitate power efficient amplifiers. Because different modulations have different features and are used in different applications and standards, a modulator that can realize more than one modulation schemes will be of great significance for a software defined radio (SDR).
For a conventional I/Q modulator structure as in Figure 2–1, different quadrature modulation schemes require different baseband processing, including pulse shaping or filtering. For example, to generate a QPSK signal, the system converts a bit stream into a Non-Return-to-Zero (NRZ) signal which is multiplied by an in-phase (I) carrier and a quadrature (Q) carrier. While for GMSK modulation, the NRZ signal needs to be passed through a Gaussian filter. Similarly, an MSK modulator would need to shape the data stream into sinusoidal pulses, whereas a QAM signal needs to be generated by varying the amplitude of the I/Q carriers. Therefore, to design a modulator circuit that can accommodate more than one schemes using the conventional I/Q approach poses considerable challenges on the digital circuit section for baseband processing.

2.2 Proposed Software Configurable Modulator

No matter what the modulation scheme is, the resulting modulated signal is essentially a carrier waveform whose phase and/or amplitude will vary according data information, pulse shaping, and baseband filtering. Therefore, precise carrier phase and amplitude control is crucial for the accuracy of any modulation. On the other hand, realizing the correct carrier phase and/or amplitude change is an alternate way of implementing a modulation. Hence, we propose such a modulator that controls the phase and/or amplitude of the carrier in order to generate a modulated signal. It will be also designed such that different controls can be applied to the modulator to allow for differently modulated signals. In other words,
we will try to make the modulator software reconfigurable and thus applicable for a software defined radio.

A simply way to view amplitude and phase is with a phasor diagram, which is exemplified in Figure 2-2, where the signal is interpreted relative to the before-modulation carrier. The modulated signal is expressed by the phasor as a magnitude and a phase. Magnitude is represented as the distance from the center and phase is represented as the angle relative to 0 degree, or I axis. The phasor’s projection onto the I axis is its “I” component and the projection onto the Q axis is its “Q” component. Amplitude modulation changes only the magnitude of the phasor, while phase modulation changes only the angle of the phasor. The magnitude and the angle of a phasor can be changed together, as in the case of QAM.
Figure 2–3. How a phasor can be generated from two phasors in quadrature

Different modulations will produce different phasor movements on the constellation. As long as the phase and amplitude changes along the constellation circle, corresponding to actual data bits, can be generated in integrated circuits, both linear and constant-envelope modulations can be implemented. As an example, Figure 2–3 illustrates how, in any particular quadrant, constant envelope and different phases, $\theta$'s, can be generated from two LO carriers in quadrature. By maneuvering the values of $a$ and $b$, which can be seen as the weights of $\cos \omega t$ and $\sin \omega t$, the two quadrature LOs, respectively, $\theta$ can be changed while $r$ maintains constant. This can be realized using a phasor combining, or summing, circuit where two quadrature LO signals are weighted and summed up to generate the in-between phasor. By choosing pairs of quadrature LOs of different phases according to the actual data, the correct quadrant on the constellation can be guaranteed.
The approach of generating an in-between phasor from two phasors in quadrature can be realized by a phasor combining circuit, or a summing circuit, whose simplified schematic can be seen in Figure 2–4. In this circuit, V1 and V2, are at carrier frequency and have a 90 degree difference in phase. I1 and I2 weigh V1 and V2 respectively, and the sum of the two weighted LOs, Vout, will be the generated phasor that falls between the two input phasors. In other words, Vout can be interpreted as a carrier signal whose phase is being changed. The amplitude of Vout, or the magnitude of the generated phasor, also depends on the values of I1 and I2. If the sum of I1 and I2 remains constant, the modulated signal will have a constant envelope. By choosing pairs of quadrature LOs of different phases according to the actual data, the correct quadrant on the constellation can be guaranteed.

This method can be applied to non-constant envelope modulations such as QAM, which utilize amplitude variations as well. In that case, both the magnitude and the angle of the phasor need to be changed, although it will make non-linear
amplification difficult. However, even if only non-linear power amplifiers are to be used, making use of techniques such as LINC (Linear Amplification with Nonlinear Components) [11], non-constant envelope modulations still can be realized with the combination of two sets of constant envelope modulators and nonlinear power amplifiers. This brings broad application prospects for modulators designed based on this principle, which essentially is just changing the phase, and possibly amplitude as well, of a carrier according to the modulation. For example, a software defined radio (SDR) can use such modulators to accommodate different modulations.

2.3 Comparison between Conventional and Proposed Modulators

As we have discussed, I/Q modulations, or quadrature modulations, are of an important role in many telecommunication applications and wireless standards. The modulator designed using the phasor combining approach is capable of generating most of the widely used I/Q modulations such as QPSK, MSK, and GMSK, but it is not exactly the same as a conventional I/Q modulator. However, different quadrature modulation schemes require different baseband processings, such as pulse shaping and filtering, which imposes challenges on the baseband circuit, especially if multiple modulation schemes are to be generated, as for an SDR [12, 13].

The phasor combining approach, on the contrary, does not require baseband processing. In principle, it directly changes the phase and/or amplitude of the carrier, according to the designated phasor movement on the constellation.
Different modulation schemes, and hence the different baseband processings they need, result in different phasor movements on the modulated signal’s constellation. Therefore, in a sense, the phasor combining approach skips the baseband processing, the analog mixing or multiplication, and the summation, and tries to create the final vector signal directly. This is done by selecting the pairs of V1 and V2 (see Figure 2–4) for correct quadrants and by controlling the weighing currents I1 and I2 for correct signal phase/amplitude. The circuitry can be much simplified in this way.

Another major difference between the two types of modulators lies in that the proposed modulator is “linear” in the sense that carrier phase and/or amplitude are changed linearly by the bias currents (I1 and I2) of the phasor combining circuit, whereas conventional I/Q modulators usually make use of devices’ nonlinearity to realize “mixing” or “multiplication”. This difference brings forth an important advantage of the phasor combining approach over the conventional I/Q modulators. Channel filtering, which is necessary for cleaning up a nonlinear modulator’s output spectrum [14, 15, 16], would not be necessary for the phasor combining modulator, making it more suitable for higher level of integration.
CHAPTER 3
DESIGN OF A TEST MODULATOR FOR FIXED PATTERNED DATA

3.1 Constant Envelope Modulation

The proposed phasor combing circuit has the potential for generating different modulation schemes by realizing different phasor change patterns in amplitude, phase, or both. Since constant envelope modulations are an important class in low power wireless communications, a constant envelope phase shift modulator circuit was built to test how well the phasor combining approach works.

Many wireless mobile products use nonlinear saturated power amplifiers because they have higher efficiency than linear amplifiers. A non-linear amplifier changes the signal amplitude by different amount depending on the instantaneous amplitude of the signal. The more the amplitude of a signal varies, the more non-linear amplification occurs, which will result in a distorted signal. Therefore, modulated signals with constant envelope are often preferred in wireless communications.

In constant envelope modulations, only phase information is employed to carry the user data, with the carrier amplitude being constant. Two examples of constant envelope modulations are Minimum Shift Keying (MSK) and Gaussian Minimum Shift Keying (GMSK). Compared to MSK, GMSK has the advantage of a more compact power spectrum due to baseband filtering, but MSK does not generate Intersymbol Interference (ISI) because the
shaping sinusoidal pulse is confined in a bit duration. In either modulation, data information is contained only in the carrier’s phase. So this type of modulations can be interpreted as phase modulation.

3.1.1 Phase Change Pattern for MSK modulation

Figure 3–1. An MSK modulation example and the modulated signal’s constellation (a) MSK modulation is I-Q modulation with half sinusoidal pulse shaping (b) The modulated signal presents a constant envelope constellation
Figure 3–2. ADS simulation for GSM

If seen from the constellation of a phase modulation signal, the signal vector, or, the phasor, changes angle according to the transmitted bits with the magnitude of the vector maintaining the same, which results in a point moving on a constant-radius circle and changing direction from time to time. This is exemplified in Figure 3–1, which shows an MSK modulation and its constellation for 8 bit intervals. The baseband I/Q channel data bits are shaped into sinusoidal pulses and respectively modulated onto two carriers with quadrature phases. Then the resulting signals of the two channels are summed up, and the modulated signal becomes a constant envelope carrier with changing phase. It can be seen that on the resulting constellation the phasor moves on a circle and changes direction based on the I/Q bit pattern. It goes over a quadrant for a one-bit interval.

3.1.2 Phase Change Pattern for GMSK Modulation

GMSK is also a constant envelope modulation scheme. It can be interpreted as a derivation from MSK in that the sinusoidal pulse shape in MSK is changed to
Gaussian. This, however, significantly complexifies the resulting modulated signal’s phase change pattern.

To investigate the phase change pattern of a GMSK signal, we used ADS simulation (Figure 3–2). This design is used to display the GMSK modulation waveform (Figure 3–3) and spectrum (Figure 3–4). The random source is GMSK modulated and the base band signal is fed to RF section which includes: RF mixer, Butterworth Filter and RF gain. Central Frequency is 935.2MHz as in GSM standard. We exported the data for the simulation result and processed it in MATLAB. Both the I-channel and the Q-channel waveform data were plotted onto an I/Q diagram to see the signal constellation (Figure 3–5). The simulation was done dynamically together with the data bits in order to observe the phase change pattern of a GMSK signal according to the data bits.

It can be seen from the simulation results that, like MSK, GMSK is also a constant envelope modulation with increased spectral efficiency, making it desirable to maximize the number of available channels. Based on the dynamic simulation from MATLAB, unlike MSK, the boundary points for a one-bit interval in GSMK, as shown in Figure 3–6, are not only the axis points anymore. Moreover, because a Gaussian pulse extends into both the previous bits and the next bits, the phase change depends on more than just two consecutive bits as in the case of MSK. The phase change pattern of GMSK can be summarized as in Table 3–1.
Figure 3–3. ADS simulated GMSK waveform (a) I-channel (b) Q-channel
Figure 3–4. ADS simulation for GMSK spectrum

Figure 3–5. MATLAB simulation of the constellation of a GMSK signal
Table 3–1. Summary of the phase change pattern of GMSK modulation

<table>
<thead>
<tr>
<th>previous two bits, current bit, next bit</th>
<th>phase change</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 or 1111</td>
<td>$A_i \rightarrow A_{i-1}$</td>
</tr>
<tr>
<td>1000 or 0111</td>
<td>$C_i \rightarrow A_i$</td>
</tr>
<tr>
<td>0001 or 1110</td>
<td>$A_i \rightarrow B_{i-1}$</td>
</tr>
<tr>
<td>1001 or 0110</td>
<td>$C_i \rightarrow B_i$</td>
</tr>
<tr>
<td>0010 or 1101</td>
<td>$B_i \rightarrow A_{i+1}$</td>
</tr>
<tr>
<td>1010 or 0101</td>
<td>$A_i \rightarrow A_{i+1}$</td>
</tr>
<tr>
<td>0011 or 1100</td>
<td>$B_i \rightarrow C_i$</td>
</tr>
<tr>
<td>1011 or 0100</td>
<td>$A_i \rightarrow C_i$</td>
</tr>
</tbody>
</table>

3.1.3 Designed Constant Envelope Phase Shift Test Modulator

MSK and GMSK can both be interpreted as constant envelope phase modulations. However, MSK has a much simpler phase change pattern, which makes it a handy choice for designing a modulator circuit to test the phasor combing approach. A test modulator circuit based on the MSK modulation was designed and fabricated in both a 0.18 µm CMOS process and a 0.13 µm process.
3.2 Design Issues Associated With the Constant Envelope Phase Shift Modulator

The designed test modulator is one that follows the phasor combining approach. It was designed for ZigBee [19] or other types of low power wireless networks. The modulator adopts an MSK-based scheme, but the phase change over any bit interval, which corresponds to a quadrant on the constellation, was implemented in a limited number of discrete steps, four in this particular design, in order to simplify the circuit architecture without compromising the performance of the modulator significantly. This will be explained in the following together with some other issue associated with the modulator design.

3.2.1 Theoretical Power Spectral Density with respect to the Number of Phase Shifts per Bit Period

A good means for checking the performance of a modulator is the modulated signal’s power spectral density (PSD). Ideal MSK modulation with randomly distributed input bits would give us a normalized PSD as shown by the solid line in Figure 3–7, which also shows the different PSDs generated from the phase shift modulation by using different numbers of phase shifts within every quadrant, starting from the axis points. It can be seen that, with one phase shift per quadrant, the PSD is the same as that of an OQPSK modulation. And as the number of phase shift steps per quadrant increases, the discrete phase shift modulation approaches MSK and the spectrum eventually becomes an MSK spectrum.
Figure 3–7. Comparison of power spectral density (PSD) with respect to the number of phase shifts per bit period. Normalized frequency is used in the figure.

As shown in Figure 3–7, the highest normalized side lobe level for the cases of 1 step, 2 steps, 4 steps per quadrant are -14 dBc, -18 dBc and -22 dBc, respectively. With four phase shifts per quadrant, the discrete phase shift modulator has a very similar spectrum as the MSK that has a -23 dBc highest side lobe level. A quadrant on the constellation corresponds to a bit period. Therefore, we chose four phase shift steps for every bit period for the design to simplify the circuit architecture.

With four phase shifts per quadrant, the output of the modulator should generate a constellation like the one in Figure 3–8, where the modulated signal moves sequentially on the circle in discrete steps and changes direction only on the I or Q axis points.
3.2.2 Impact of Variations in the Modulated Signal’s Amplitude and Phase Shift Step

The results in Figure 3–7 were simulated by assuming an ideal modulator that produces constant amplitude and constant phase shift step size. However, due to a summing circuit’s gate-to-drain RF feedthrough of the two quadrature input signals, which exists even when one of the two summing weights is set to zero, perfect constant amplitude within each quadrant of the modulated signal’s constellation cannot be achieved by real circuit. The size of the phase shift steps also varies across the constellation. The variation in the modulated signal’s amplitude and phase shift step will lead to deviation of the signal point from the ideal symbol point on a constellation, which will increase the EVM of the modulator. The EVM (Error Vector Magnitude) is the difference between the ideal vector convergence point and the transmitted point on a signal constellation. It
is defined as the rms value of the error vectors in relation to the magnitude of an ideal symbol. It is obvious that the bigger the amplitude/phase shift variations are, the worse the modulator will perform in terms of EVM. Meanwhile, we also need to investigate the impact on the output spectrum.

In order to take into account more and different variations of the modulated signal, the effect of the variance of variations in the output signal’s amplitude, or in its phase shift among the four steps within each quadrant, was further studied. That is, we treated the variation as a random variable, with a mean of zero and an approximated variance based on the data from simulation results, and studied the relationship between the modulator’s performance, in terms of sidelobe level, and the variance of the variation (VOV). We denoted VOV as $\sigma_V^2$.

For example, based on probability theory, the VOV in phase shift can be approximated as

$$\sigma_V^2 = \frac{1}{4} \sum_{i=1}^{4} [(\hat{\phi}_i - \phi_i) - (\hat{\phi}_i - \phi_i)]^2$$

(3-1)

where $\phi_{i=1:4} = 0, \pi/8, \pi/4, 3\pi/8$ and $\hat{\phi}_i$'s are actual values of implemented phases. To simulate the effect, four normally distributed random values with zero mean and variance of $\sigma_V^2$ were generated to represent the variations from the four ideal phase points in a quadrant. Figure 3–9 plots the first sidelobe level normalized to mainlobe level (dBc) versus the different values of $\sigma_V$ in phase shift. For the modulator design, maximum angle deviation from the ideal phasor can be looked up in Figure 3–9 as the worst case scenario in terms of phase shift variation to see how the performance will be affected. The results shown in Figure 3–9 indicate
Figure 3–9. Normalized sidelobe level (referenced to mainlobe level) versus variations in amplitude and phase shift (The X-axis has a unit of radians for phase shift variation, and it indicates percentage for amplitude variation)

that, if $\sigma_V$ is less than 0.1 radian ($5.73^\circ$), the increase of sidelobe level from the ideal case is less than 1dB.

Figure 3–9 also plots the effect of amplitude variation on the PSD’s sidelobe increase. The effect appears to be similar to that of phase shift variation. Note that the X-axis has a unit of radians for phase shift variation, and it indicates percentage for amplitude variation. Therefore, when $\sigma_V$ in the amplitude of the modulation is less than 10%, or when $\sigma_V$ in the phase shift step is less than 0.1 radian, the modulator’s performance will not be degraded significantly. It should be pointed out, however, that the variation in the amplitude of the modulated signal is likely to disappear after the signal is amplified by a non-linear and saturated power
amplifier (PA). Therefore, it should not be a critical factor for the performance of the modulator when integrated in a transmitter with a non-linear PA.

### 3.3 Circuit Description

As discussed earlier, the modulator design is based on the MSK modulation scheme, but MSK’s continuous phase change over each bit interval is implemented in four discrete steps. Figure 3–10 specifically illustrates how the four discrete phases within a quadrant, or the four phasors (P0, P1, P2, P3), can be generated from two quadrature phasors sin\(\omega t\) and cos\(\omega t\). Table 3–2 lists the four pairs of summing weights (a and b) for generating the four phasors.

Table 3–2. Summing weights for generating different phasors

<table>
<thead>
<tr>
<th>Phasor</th>
<th>P0</th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase ((\theta))</td>
<td>0</td>
<td>(\frac{\pi}{8})</td>
<td>(\frac{\pi}{4})</td>
<td>(\frac{3\pi}{8})</td>
</tr>
<tr>
<td>Summing Weight (a)</td>
<td>(\propto) cos 0</td>
<td>(\propto) cos (\frac{\pi}{8})</td>
<td>(\propto) cos (\frac{\pi}{4})</td>
<td>(\propto) cos (\frac{3\pi}{8})</td>
</tr>
<tr>
<td>Summing Weight (b)</td>
<td>(\propto) sin 0</td>
<td>(\propto) sin (\frac{\pi}{8})</td>
<td>(\propto) sin (\frac{\pi}{4})</td>
<td>(\propto) sin (\frac{3\pi}{8})</td>
</tr>
</tbody>
</table>
A block diagram of the constant envelope phase shift modulator circuit is shown in Figure 3–11. The circuit is mainly composed of a 2:1 divider, two 4:1 differential multiplexers, a phasor combining circuit (summing circuit), output buffers, and a digital circuit section to control these blocks.

### 3.3.1 Divider

From a differential 2xLO (twice the LO frequency) input signal, a 2:1 current mode logic static frequency divider, as shown in Figure 3–12, generates four signals with phases that are equally separated over 360 degrees, as indicated by the four crosses on the I/Q axes in Figure 3–8. The divider has a differential master-slave configuration. The inverted slave outputs are connected to the master inputs. The cross connection between the slave and the master generates an output frequency at half of the input (CLK and CLKb) frequency. The differential output from the master (Qi and Qbi) is in quadrature with that of the slave (Q and Qb). Therefore,
Figure 3-12. A 2:1 static frequency divider (a) Block diagram (b) A detailed divider schematic

with a differential input at a frequency twice the designated LO frequency for the modulation, the divider will provide four LO signals whose phases are 90 degrees apart from one another. Both the master and the slave consist of two input transistors (M1 and M2), two drive transistors (M4 and M5), two latch transistors (M3 and M6), and two load transistors (M7 and M8). The self-oscillation frequency of a divider increases as the sizes of the transistors are decreased, although driver transistor size has less effect that the sizes of other transistors [20]. At a given
drive transistor size, the smaller the latch transistors’ size is, the lower the output voltage amplitude gets [20]. However, increasing transistors’ size will also increase power consumption. Due to these tradeoffs, and since the divider must be designed based on the acceptable power consumption and output signal level, the chosen transistor sizes will set a limit on the operating frequency of the divider. The operating frequency range of the divider will determine the modulator’s operating bandwidth to a great extent.

### 3.3.2 Multiplexers

From the four LO signals generated by the divider, two 4:1 differential multiplexers (MUXes) are used to select the present state and the next state. The two states correspond to the two boundary points of a quadrant on the I/Q plane, whereby the modulated signal phase would change by 90 degrees during any bit interval. The selected pair of the two states holds for a bit interval before being changed by the two 4:1 MUXes for the next bit interval. Each 4:1 MUX is designed to consist of two stages of 2:1 differential MUXes. The two stages are controlled by two clocks, Clock1 and Clock2, respectively, as can be seen from Figure 3–11. One of the two clocks, Clock1 in this design, controls the bit rate, and the other clock embeds the digital data bits. Figure 3–13 shows the schematic of a 2:1 current-steering MUX [14] used in the design. This structure allows for a reduced voltage swing. Simulations also indicate that switching of the current can be performed at a speed higher than switching of the voltage [14]. Therefore this type of MUX can increase the operating speed of the circuit, which allows for
higher data rates, especially if the same circuitry is to be used for implementing different modulation schemes.

Compared to a one-stage 4:1 MUX [15], the two-stage configuration, although more complex, suffers less speed penalty and maintains fully-differential signals better [16]. Both configurations require at least two inputs, one for the clocks, and the other for data, which will decide what to select from the four LO signals. Simulation result also showed that, for this modulator design, the power consumption of using two-stage MUXes was not significantly higher than using one-stage ones.

Figure 3–13. A 2:1 differential current-steering multiplexer
3.3.3 Phasor Combining Circuit

After passing through buffers, the present state signal and the next stage signal are fed into a phasor-combining circuit, which is shown in Figure 3–14. The phasor-combining circuit sums the input signals to produce a signal with a phase shifting between those of the two inputs. Different intermediate phases can be generated by applying different bias currents ($I_1$ and $I_2$) as summing weights, which can be realized by using digital logic circuits to switch the current sources. As can be seen from Figure 3–14, three switches, which turn on or off the three bias current sources $I_{b1}$, $I_{b2}$, and $I_{b3}$, are controlled by digital circuit to generate four different combinations of $I_1$ and $I_2$ values within a bit interval, in order to implement the four intermediate phase shifts within any particular quadrant period. The digital control signals for switch 1 and switch 3 are differential and
thus neither $I_b1$ nor $I_b3$ will contribute to $I_1$ or $I_2$ at the same time, while $I_b2$ always contributes to $I_1$ only. The controls of the switches are designed such that the four combinations of $I_1$ and $I_2$ are as follows.

1) $I_1 = I_b1 + I_b2 + I_b3 \propto \cos 0^\circ, I_2 = 0 \propto \sin 0^\circ$ (to generate a $0^\circ$ phase shift relative to the present state);

2) $I_1 = I_b2 + I_b3 \propto \cos 22.5^\circ, I_2 = I_b1 \propto \sin 22.5^\circ$ (to generate a $22.5^\circ$ phase shift);

3) $I_1 = I_b1 + I_b2 \propto \cos 45^\circ, I_2 = I_b3 \propto \sin 45^\circ$ (to generate a $45^\circ$ phase shift);

4) $I_1 = I_b2 \propto \cos 67.5^\circ, I_2 = I_b1 + I_b3 \propto \sin 67.5^\circ$ (to generate a $67.5^\circ$ phase shift).

$I_1$ and $I_2$ weigh the present state signal and the next state signal respectively, and $V_{out}$ is the sum of the two weighted signals, with an in-between phase. In the meantime, constant amplitude of $V_{out}$ can be maintained by keeping the sum of $I_1$ and $I_2$ constant ($I_b1 + I_b2 + I_b3$).

### 3.3.4 Buffers

The last stage of the modulator design is an output buffer/amplifier to drive 50 $\Omega$ single-ended loads for the purpose of testing with 50 $\Omega$ instruments. Three buffers similar to the one in Figure 3–15 are cascaded to serve as the driver. The buffers use resistor loads to achieve a broadband response. There is also a buffer stage between the MUXes and the phasor combining circuit.
3.3.5 Digital Circuit Section

As introduced earlier, the modulator circuit needs many clock signals (e.g., for the MUXes) and control signals (e.g., for controlling the switches of the phasor combining circuit). For testing purpose, the modulator chip is designed with only one clock input, and all the clocks and controls are generated by digital circuitry on the chip. Because these signals are of relatively lower frequencies, CMOS logic digital circuit is used for lower power consumption. The digital circuit section consists mainly of two sets of the combination of master-slave flip-flops and XOR gates, with one set generating the control signals for the switches, and the other generating the clocks for the MUXes. The two sets are separately configured and connected according to the desired waveforms of the clocks and the controls. In both sets, the masters and the slaves use the same type of flip-flop latch as
shown in Figure 3–16 [21]. Latches are also used to line up the correct edges of the generated clocks and controls.

3.4 Experimental Results

3.4.1 Modulator IC Fabricated in 0.18 μm CMOS Process

The modulator IC was designed and fabricated in a 0.18 μm mixed signal CMOS process with a supply voltage of 1.8 V. The chip, which we will call the 0.18 μm chip for the convenience of discussion, occupies an area of 0.5 mm². Its microphotograph is shown in Figure 3–17.

In designing this particular modulator testing chip, repetitive data pattern was internally generated and translated into the multiplexers, creating a modulated signal that moves clockwise in circles at a constant speed, determined by the data rate, on the constellation. The purpose was twofold: 1) to reduce the spectrum bandwidth of the output signal so that it can be measured by equipment with limited bandwidth; 2) to simplify testing the IC without the need for a high-speed
Figure 3–17. Die microphotograph of the modulator IC (0.18 µm chip)

data pattern generating instrument or multiple high frequency clock signal sources. In this design, only an RF signal input, for the divider to generate the four phased LO signals, and a single clock input, for controlling the MUXes and timing the internal digital circuits, are needed.

To derive the mathematical description of a signal modulated in such a way, assume that the carrier is in the form of $A \cos(2\pi f_c t + \phi_0)$, where $A$ is the amplitude of the carrier, $f_c$ is the carrier frequency, and $\phi_0$ is the initial phase of the carrier. Without loss of generality, $\phi_0$ can be assumed to be zero. A modulated signal moving clockwise on the constellation circle continuously means that the carrier’s phase decreases continuously with time. Denote the bit rate as $R$ and therefore the bit interval $T = 1/R$. Since the phase change of an MSK signal within a bit
interval, $T$, is $\pi/2$, the modulated signal, $s(t)$, can be expressed as

$$s(t) = A \cos\left(2\pi f_c t - \frac{\pi/2}{T} t\right)$$  \hspace{1cm} (3-2)$$

$$= A \cos\left(2\pi f_c t - \frac{\pi}{2} R t\right)$$  \hspace{1cm} (3-3)$$

$$= A \cos\left[2\pi \left(f_c - \frac{1}{4} R\right)t\right].$$  \hspace{1cm} (3-4)$$

Therefore, $s(t)$ is still a single tone sinusoidal signal, but its frequency is $\frac{1}{4}R$ lower than the original carrier frequency. Because in this design the continuous phase change is implemented in four discrete steps, the mathematical expression for the actual signal, $s_a(t)$, should instead be

$$s_a(t) = A \cos\left(2\pi f_c t - \frac{\pi}{8} \left\lfloor \frac{t}{T/4} \right\rfloor\right),$$  \hspace{1cm} (3-5)$$

where $\lfloor \cdot \rfloor$ is the floor operator, which gives the largest integer less than or equal to the operand. MATLAB simulation was performed to estimated the output spectrum of $s_a(t)$, which is shown in Figure 3–18.

The modulator IC was tested using an Agilent 89600 series Vector Signal Analyzer (VSA) with an external power amplifier connected to the output of the chip. The VSA has a bandwidth of 36 MHz. From the measured spectrum of the modulator’s output signal in Figure 3–19, it can be seen that it matches the theoretical estimation. The bit rate was set to 100 Mbps in the measurement, the carrier frequency was 2.5 GHz, and the spectrum shows a single tone with the center frequency at 2.475 GHz which is exactly 25 MHz lower than the carrier frequency. It should be pointed out that, although fixed data pattern was
Figure 3–18. Simulated output power spectrum for the fixed repetitive data pattern.

Figure 3–19. Measured output power spectrum. Signal's frequency is 25 MHz, or one fourth of the 100 MHz bit rate, lower than the 2.5 GHz carrier frequency.
Figure 3–20. Measured constellation (0.18 µm chip) of the modulated signal (EVM = 2.8%). The signal moved sequentially and repetitively in full circles designed and used to simplify the measurement, at the end of every bit interval the multiplexers always re-select two LOs in quadrature as the new “present” and “next” states. Therefore, the data rate of the fixed pattern data still signifies the bit rate that the modulator can manage for arbitrary data patterns. As observed in the measurement, as the data rate increased (the signal vector rotated clockwise faster), the frequency shift in output spectrum also increased.

Figure 3–21. Measured I/Q plane diagram (0.18 µm chip) of the modulated signal

Figure 3–20 shows a constellation measured using Agilent 89600 Vector Signal Analyzer (VSA), with an external power amplifier connected to the 0.18 µm
chip’s output. This test was used to verify the correctness of the phase shifts. The I/Q plane diagram in Figure 3–21 demonstrates the constant envelope feature of the modulator. The bit rate was set to 100 Mbps in the measurement. The measurement result showed an average EVM (Error Vector Magnitude) of 3%.

With one of the differential outputs terminated by 50 Ω, the 0.18 µm test chip delivered a signal level of -2 dBm to a 50 Ω load. The modulator was designed for low power applications, and the measured current dissipation was 2 mA with the supply voltage being 1.8 V. It should be noted that this current dissipation did not include that of the three cascaded output buffers, which, although consumed 10 mA current, are not necessarily an integral part of the modulator, if the modulator is put into a transmitter chain and only needs to drive the input impedance of the next stage circuit such as an mixer or a power amplifier.

Figure 3–22. Measured EVM vs. carrier frequency (0.18 µm chip). At 100 Mbps bit rate, for EVMs lower than 5.5%, the modulator can operate at a carrier frequency between 1.75 GHz and 3.5 GHz.
The frequency range of the carrier was also measured. The measurement was done by keeping the bit rate fixed at 100 Mbps and monitoring the signal constellation and EVM while changing the RF input frequency which is twice the LO carrier frequency. As can be seen from Figure 3–22, within the carrier frequency range of 1.75 GHz to 3.5 GHz, the modulator works fine with lower than 5.5% EVMs (The IEEE 802.11a standard [22] specifies a maximum EVM of 5.62% for the peak data rate of 54 Mbps.). Another measurement was done to find out the bit rate the modulator circuit can handle with a 2.5 GHz carrier. The resulting EVMs at different bit rates are plotted in Figure 3–23. Although a 500 Mbps bit rate can turn in a decent EVM of 5%, measurement showed that higher bit rate would result in blurry constellation (see Figure 3–24) and degraded EVM (greater than 6%), if the carrier frequency remained the same.
Figure 3–24. Constellation (EVM = 6%) at bit rate greater than 500 Mbps (0.18 μm chip)

Figure 3–25. When the error vector is perpendicular to the ideal phasor, the phase variation is the biggest

EVM is a direct measure of the accuracy of a modulator. The contributors to the degradation in EVM could include variations in phase and amplitude, phase noise, poor frequency response at any stage of the system, poor return loss, and virtually any other RF system related problems. At a certain EVM value, the maximum possible phase variation, ΔΦ, occurs in the case of Figure 3–25, where the error vector is perpendicular to the ideal phasor. For EVM = 6%, ΔΦ approximately equals 0.085 radian. According to Figure 3–9, this variation will not affect the PSD significantly. Same analysis can be applied to the amplitude
When the error vector is in the same direction as the ideal phasor, the amplitude variation is the biggest variation, where the worst case scenario is as in Figure 3–26. Again, at a 6% EVM, the variation in amplitude has little impact on the modulator's output PSD, especially considering that the signal will be amplified through an amplifier in saturation.

A brief performance summary for the constant envelope phase shift modulator (0.18 μm chip) is listed in Table 3–3.

Table 3–3. Summary of modulator performance (0.18 μm chip)

<table>
<thead>
<tr>
<th>Function</th>
<th>Constant envelope phase modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18 μm CMOS</td>
</tr>
<tr>
<td>Die size</td>
<td>0.5 mm²</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Current dissipation (excluding output buffers)</td>
<td>2 mA</td>
</tr>
<tr>
<td>EVM</td>
<td>2.8% (at 2.5 GHz and 100 Mbps)</td>
</tr>
<tr>
<td>Carrier frequency range</td>
<td>1.75 GHz to 3.5 GHz</td>
</tr>
<tr>
<td>Bit rate</td>
<td>DC to 500 Mbps</td>
</tr>
</tbody>
</table>

3.4.2 Modulator IC Fabricated in 0.13 μm CMOS Process

The modulator design was also fabricated in a 0.13 μm logic CMOS process with a supply voltage of 1.2 V. The schematic of the complete modulator test chip circuit in the 0.13 μm process is shown in Figure 3–27. The microphotograph of the 0.13 μm chip is shown in Figure 3–28. The 0.83 mm² chip size is considerably bigger than the 0.18 μm chip, because more pads for DC biases were placed on this
Figure 3–27. Complete modulator test chip circuit (0.13 µm chip)
chip for the purpose of separately controlling of the three stages of output buffers and adjusting the amplification gains. The reason for more controls and biases is that big metal capacitors, whose parasitic values are high, were used in the layout as inter-stage coupling capacitors because no MIMCAPs are available in a logic process.

Figures 3–29 and 3–30 are the measured constellation and the I/Q plane diagram, respectively, of the 0.13 µm chip’s output. The measurement setup was almost the same as for the 0.18 µm chip, except that more DC power supplies were used for output buffer bias control. At a carrier frequency of 2.5 GHz and a bit rate of 100 Mbps, the measured EVM was 3.5%.
The 0.13 µm test chip also has a measured current dissipation of 2 mA (excluding output buffers) with the supply voltage being 1.2 V, so the power consumption was even smaller than the 0.18 µm chip. The operating carrier frequency (at a 100 Mbps bit rate) ranges from 1.5 GHz to 3.3 GHz, with the measured EVMs all equal to or below 4% (Figure 3–31). However, the maximum bit rate appeared to be much lower than the 0.18 µm chip, as can be seen from Figure 3–32. At a 250 Mbps data rate, the EVM value is already 6.5%, with the carrier frequency maintaining the same at 2.5 GHz. Compared to the previous chip, the smaller operating frequency range and bit rate range are probably caused by the coupling capacitors used in the layout. Big metal capacitors with considerably higher parasitic values were used instead of MIMCAPs, which led to higher inter-stage power loss in the circuit. Therefore, the output signal level decreased, degrading SNR and hence EVM. A performance summary for 0.13 µm modulator test chip is listed in Table 3–4.
Figure 3–30. Measured I/Q plane diagram (0.13 µm chip) of the modulated signal

Table 3–4. Summary of modulator performance (0.13 µm chip)

<table>
<thead>
<tr>
<th>Function</th>
<th>Constant Envelope Phase Modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.13 µm CMOS</td>
</tr>
<tr>
<td>Die size</td>
<td>0.83 mm²</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Current dissipation</td>
<td>2 mA</td>
</tr>
<tr>
<td>EVM</td>
<td>3.5% (@2.5 GHz and 100 Mbps)</td>
</tr>
<tr>
<td>Carrier frequency range</td>
<td>1.5 GHz to 3.3 GHz</td>
</tr>
<tr>
<td>Bit rate</td>
<td>DC to 225 Mbps</td>
</tr>
</tbody>
</table>

3.4.3 Performance Comparison

From the experiment results of both modulator test chips, it can be seen that, in addition to the functionality and the low power consumption, the modulators of this work work at a big range of operating frequency and high data rates. Table 3–5 compares this work to some of the reported modulators of similar functions.
Figure 3–31. Measured EVM vs. carrier frequency (0.13 µm chip). At 100 Mbps bit rate, for EVMs lower than 4%, the modulator can operate at a carrier frequency between 1.5 GHz and 3.3 GHz.

Figure 3–32. Measured EVM vs. bit rate (0.13 µm chip). At 2.5 GHz carrier frequency, for EVMs lower than 5.5%, the bit rate of the modulator ranges from DC to 225 Mbps.
Table 3–5. Comparison of modulator performance

<table>
<thead>
<tr>
<th>Reported modulators</th>
<th>Power consumption (mW)</th>
<th>Operating frequency range (GHz)</th>
<th>Bit rate (Mbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Devices AD8349</td>
<td>675</td>
<td>0.7-2.7</td>
<td>0-160</td>
</tr>
<tr>
<td>MITEQ SDM6474LCDQ</td>
<td>1800</td>
<td>6.4-7.4</td>
<td>0-100</td>
</tr>
<tr>
<td>CMOS I/Q modulator #1 [23]</td>
<td>175</td>
<td>2.4</td>
<td>11</td>
</tr>
<tr>
<td>CMOS I/Q modulator #2 [24]</td>
<td>187.8</td>
<td>1</td>
<td>3.75</td>
</tr>
<tr>
<td>this work</td>
<td>3.6</td>
<td>1.75-3.5</td>
<td>0-500</td>
</tr>
</tbody>
</table>
CHAPTER 4
A DIGITALLY CONTROLLED PHASE SHIFT MODULATOR FOR ARBITRARY DATA PATTERNS

Constant envelope modulations, such as MSK and GMSK, allow the power amplifier (PA) to be operated in saturation, and can achieve greater efficiency than linear modulations. The test modulator introduced in the previous chapter can generate a constant envelope modulated signal, and therefore can be used in a low power transmitter utilizing a non-linear PA, such as a Class B or a Class C PA.

The standalone test modulator introduced in the previous chapter only accommodate a fixed data pattern, which results in a signal point moving sequentially in the same direction in full circles on the constellation. The reasons for that design were that it can simplify the digital circuitry to some extent and that measurement will be relaxed in terms of the requirementS for equipment, because a random or pseudo random data generator would not be necessary.

But to be integrated in a transmitter, the modulator should be able to take arbitrary input data and modify them onto the carrier. Therefore, the previous modulator circuit was modified accordingly, with no major changes made to the architecture.

4.1 Design Details

The test modulator for fixed patterned data, which was an internally generated clock signal and translated into a phasor moving repetitively and sequentially in
circles on the constellation as introduced in the previous chapter, has been proved to have very good performance. Therefore, the design of a modulator for arbitrary data should be aimed to involve minimal modification. Hence, the fundamental circuit architecture of this modulator for arbitrary data patterns remains the same as the test modulator, except that the clock generation and digital control circuit needs to be modified in order to take the input of serial digital data bits. However, the internal clocks for timing the multiplexers and for controlling the switches of the phasor combining circuit are still generated from one external clock input.

Let us take a look back at the example of an MSK signal in the previous chapter. In Figure 3–1(a), the serial digital data bits are 10110010 before being converted to two parallel data streams (I stream 1101 and Q stream 0100). The resulting phasor movement can be seen in Figure 3–1(b) and is redrawn here in Figure 4–1 for convenience of discussion. It should be noted that A, B, C, and D in this figure are the four boundary phase points for the bit intervals. The signals with these four phases can be generated at the output of the divider, as can be seen in Figure 3–27.

As explained in the previous chapter, the modulator circuit needs to select the correct boundaries for each bit interval, which is to be done by the two 4:1 MUXes. Because the phasor would move from one boundary point to an adjacent other one during each bit interval, two boundary points (starting point and ending point) need to be selected by the two MUXes respectively, which is what is meant by the “present” state and the “next” state in the previous description of the modulator circuit. For this 8-bit-interval MSK example, Figure 4–2 shows the boundary points
Figure 4–1. Movement of the phasor when serial data stream 10110010 is MSK modulated

Figure 4–2. Boundary phases on the constellation for the 8 bit intervals
Figure 4–3. How a state stream can be generated at the output of a MUX at the 8 bit intervals. For these 8 intervals, the starting points, or the “present” states, which are to be selected by one of the two MUXes, are $A, B, A, D, C, B, A$, and $B$, while the ending points, or the “next” states, which are to be selected by the other MUX, are $B, A, D, C, B, A, B$, and $C$. The ending point of the $8^{th}$ bit interval $C$ will be the starting point of the $9^{th}$ should there be one. For discussion purpose, the output of an MUX for a series of bit intervals is called state stream. It can be seen that, the phase streams at the two MUXes’ output are the same, except that the MUX for the “present” states generates a state stream that is delayed by one bit interval, compared to the state stream generated by the MUX for the “next” states.

Figure 4–3 illustrates how a 4:1 MUX is designed and controlled to select the correct phase states according to the input serial data bits. Note that the “clock” here is not the clock input to the entire chip but rather one that is generated.
therefrom. As in the previous design, “clock” is internally generated by the on-chip digital circuit section and its rate is twice the rate of serial data. This MUX can be used for the “next” state stream, while for the “present” state stream, both “clock” and “data” are delayed by one bit interval using a flip-flop latch as in Figure 3–16. Efforts also need to be made to ensure the edges of the digital data bits and the clocks are lined up.

The block diagram of the modified modulator for arbitrary data patterns is shown in Figure 4–4. It can be seen that the main architecture of the modified modulator for arbitrary data patterns remains the same as the one with a fixed data pattern. The continuous phase change of MSK within any quadrant is still implemented in four discrete steps. With pseudo random input data bits, the ideal normalized output power spectral density (PSD) will be the one in Figure 3–7 for the case of 4 phase shifts per quadrant. We can take it out and show it in Figure 4–5. The ideal constellation for MSK modulated random data is a constant envelope circle, with four data points each in one quadrant, as in the case of QPSK/OQPSK. Figure 4–6 illustrates what the constellation will look like.

4.2 Experimental Results

The modulator circuit for arbitrary data patterns was fabricated in a 0.18 μm mixed signal CMOS process. The microphotograph of the chip is shown in Figure 4–7. The area of the chip is 0.677 mm².

Figure 4–8 shows the measurement setup for testing the modulator circuit with pseudo random input data bits. The signal generator provides an AC signal
Figure 4–4. Modulator circuit for arbitrary data patterns

Figure 4–5. Ideal normalized output PSD for the modified modulator if pseudo random input data are applied
Figure 4–6. Ideal constellation for the modified modulator if pseudo random input data are applied

Figure 4–7. Die microphotograph of the modulator circuit for arbitrary data patterns
Figure 4–8. Measurement setup for testing the modulator circuit with pseudo random input data bits whose frequency is twice the desired carrier frequency, or LO frequency, for the modulator. The on-chip 2:1 frequency divider will generate four LOs whose phases are in quadrature with one another. Agilent N4906A bit error rate tester (BERT) is used to provide the circuit with data and clock inputs. It should be noted that the BERT data output has the same rate as its clock output, while the actual modulator circuit needs an input clock rate that is four times the input data rate because the input clock will be used to generate all the on-chip clock and control signals, including the “clock” signal in Figure 4–4. However, the measurement is feasible using the BERT despite its seemingly wrong data rate, because the input data bits to the modulator are being latched by flip-flops at the rate of one of the internally generated clocks, which is the desired data rate. Therefore, the flip-flops act like a sampler which samples the higher-rate data input at the desired data rate which the circuit needs. The BERT can generate hardware based pseudo random
Figure 4-9. Measured constellation at 2.5 GHz carrier frequency and 12 Mbps bit rate

bit streams (PRBS) up to $2^{23} - 1$, therefore the actual sampled data into the modulator circuit are a PRBS of $2^{21} - 1$ because the data rate after sampling is one fourth the rate of the BERT’s data output. The modulator’s differential output signal is measured by terminating one end with 50 Ω and externally amplifying the output of the other end. The amplified signal is connected to a spectrum analyzer and a VSA hardware via a power splitter. The VSA hardware is connected to a PC where the VSA software is installed. The modulated signal will be down-converted and sampled by the VSA hardware and demodulated by the VSA software. The demodulated signal’s constellation and I/Q diagram can be displayed on the PC’s monitor.

The Agilent 89600S VSA is limited to a bandwidth of 36 MHz by its digitizer. Therefore, the data rate of a modulated signal it can measure is also limited. To accurately demodulate a signal, ideally all the sidelobes in the spectrum should be
Figure 4–10. Measured I/Q diagram at 2.5 GHz carrier frequency and 12 Mbps bit rate

included in the frequency span of the VSA. Since the lowest output clock/data rate of the BERT is 48 MHz, the modulator was measured at 2.5 GHz carrier frequency and 12 Mbps bit rate. Figure 4–9 and Figure 4–10 show the measured constellation and I/Q diagram respectively. At this carrier frequency and bit rate, the average measured EVM was 7%.

Figure 4–11 shows the power spectrum of the modulated signal measured by a spectrum analyzer, and it can be seen that the measured result is quite similar to the simulation result in Figure 4–5. Figure 4–12 allows for a closer look at the mainlobe and its adjacent sidelobes of the measured spectrum. It can be seen that the measured mainlobe width is approximately 18 MHz, which is 1.5 times the bit rate, and the first sidelobes are about 12 MHz, which is one bit rate, away from the center frequency. These are consistent with the simulation result in Figure 4–13.
The measured power spectra at some higher bit rates can be seen in Figure 4–14 and Figure 4–15, where the bit rates are 50 Mbps and 100 Mbps, respectively, while the carrier frequency remains the same at 2.5 GHz. The output signal’s power level is around -3 dBm. Note that for these measurement results the resolution bandwidth of the spectrum analyzer was set to 3 MHz. The power consumption of this modified modulator is the same as the previous modulator with the fixed data pattern. That is, the modulator without the output buffers to drive 50 Ω loads dissipates 2 mA current, while the output buffers need a total of nearly 10 mA bias current.

This modified modulator circuit for arbitrary data patterns is a great candidate to be used for personal area networks complying with the ZigBee technology. The IEEE 802.15.4 standard [25], which a ZigBee-ready transceiver should be compliant to, is designed for low cost, low power consumption wireless
Figure 4–12. Measured power spectrum with a smaller frequency span at 2.5 GHz carrier frequency and 12 Mbps bit rate

Figure 4–13. Simulated power spectrum of the modulator output with pseudo random input data bits
Figure 4–14. Measured power spectrum at 2.5 GHz carrier frequency and 50 Mbps bit rate

Figure 4–15. Measured power spectrum at 2.5 GHz carrier frequency and 100 Mbps bit rate
applications with moderate data rates. The standard specifies the Physical (PHY) and Media Access Control (MAC) layers at the 868 MHz, 915 MHz and 2.4 GHz ISM bands, and the chip modulation schemes are O-QPSK with half-sine pulse shaping (MSK) for 2.4 GHz PHY and BPSK with raised cosine pulse shaping for 868/915 MHz PHY, respectively. The layers of the IEEE 802.15.4 standard and ZigBee technology are shown in Figure 4–16 [26]. The 2.4 GHz PHY of the IEEE 802.15.4 standard is more attractive to the wireless industry because the 2.4 GHz unlicensed ISM band is globally available and therefore flexible in application designs [26]. The chip rate for the 2.4 GHz PHY is 2 Mchips/s from a data rate of 250 kbps, and the specified EVM requirement is 35%. The average EVM result of this modulator at 2.5 GHz carrier frequency and 12 Mbps bit rate is 7%, and the recorded worst-case EVM value is around 10%, which is still well below the requirement limit.
Figure 4–17. Output spectrum of the CC2420 transmitter

Figure 4–17 shows the output power spectrum of the CC2420 transmitter [26]. The CC2420 is a low-cost transceiver designed for low-power, low-voltage RF applications in the 2.4 GHz ISM band. It is a ZigBee-ready CMOS device using a mainstream 0.18 \( \mu \)m technology. As can be seen from its output spectrum, the mainlobe occupies a bandwidth of approximately 3 MHz, which is twice the 2 Mchip/s chip rate in the IEEE 802.15.4 specification. The modulated signal transmitted by the CC2420 has a worst-case EVM of 20% [26]. Therefore, the modulator circuit of this work surpasses the performance of the CC2420 in terms of transmit modulation accuracy. It also supports much higher data rate than the CC2420.
The performance of the modulator circuit for arbitrary data patterns is summarized in Table 4–1.

Table 4–1. Performance summary of the modulator for arbitrary data patterns

<table>
<thead>
<tr>
<th>Function</th>
<th>Constant Envelope Phase Modulation (MSK-like)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18 µm CMOS</td>
</tr>
<tr>
<td>Die size</td>
<td>0.677 mm²</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Current dissipation (excluding output buffers)</td>
<td>2 mA</td>
</tr>
<tr>
<td>EVM</td>
<td>7% (@2.5 GHz and 12 Mbps)</td>
</tr>
</tbody>
</table>
CHAPTER 5
DESIGN OF A DIRECT CONVERSION TRANSMITTER

In the previous chapter, we introduced a digitally controlled phase shift modulator circuit for an MSK-like modulation scheme, which is suitable for ZigBee-ready IEEE 802.15.4-compliant devices. Such devices, as the standard is designed for, are expected to be low cost and low complexity. In addition, the compliant system implementations will enable long battery life by using the power-saving features at the PHY, MAC, and network layers specified by the standard [26].

In addition to the functionality of the modulator, we also wanted to demonstrate the modulator’s suitability for high level integration. Therefore, we integrated the modulator circuit into a direct conversion transmitter, which will be introduced in the following sections.

5.1 Direct Conversion Transmitters

Many factors, such as function, power consumption, ease of integration, and requirement of external components, can affect the choice of a specific transmitter architecture for a specific standard and application. To comply with the low-cost low-power nature of the IEEE 802.15.4 standard, the direct conversion transmitter architecture is the best fit for efficient generation of the transmit signal.

Direct conversion transmitters appeal to designers of wireless systems for their simplicity and low cost. The direct conversion architecture eliminates the
Figure 5–1. Generic direct conversion transmitter utilizing the conventional I/Q modulator

Intermediate frequency (IF) stage and its accompanying IF surface acoustic wave (SAW) filter, mixer, and voltage-controlled oscillator (VCO) components. Fewer parts means lower total cost, smaller devices and greater reliability. It also means less insertion loss and less power consumption. Although a superheterodyne transmitter is generally considered a higher-performance transmitter, if the system requirements can be met with the direct conversion transmitter, which is more suitable for high levels of integration, then a more economical radio can be realized.

In direct conversion transmitters, modulation is done directly to the carrier at the designated output frequency and an upconversion is not needed. A simple direct conversion transmitter generally consists of an oscillator, a modulator, and power amplifiers, while a complicated one would include a phase-locked oscillator. Figure 5–1 [27] shows a simplified block diagram of a generic direct conversion transmitter utilizing the conventional I/Q modulator as we introduced previously.
It can be seen that the transmitter includes baseband processing and analog mixing through two mixers. The digitally controlled constant envelope phase modulator of this work has the function of realizing the I/Q modulation schemes. It also has many advantages over the conventional I/Q modulators. Therefore, we incorporated this modulator into the design of the direct conversion transmitter, whose block diagram is shown in Figure 5–2. In this design, a VCO will generate a signal at twice the designated carrier frequency, which will be divided down by a 2:1 frequency divider to the output RF frequency of the transmitter. The output signal from VCO will be connected to the modulator for arbitrary data patterns, where four signals whose phases are in quadrature with one another will be generated from the VCO’s output by the 2:1 frequency divider. The output of the modulator will be an MSK-like modulated signal with a constant envelope, which allows for the use of a simple low-cost and relatively non-linear succeeding power amplifier (PA). It should be pointed out that no baseband processing is needed in this transmitter architecture. With a VCO preceding the modulator, and a PA following it, the modulator can be easily placed into a direct conversion transmitter chain. The blocks after the PA, such as the antenna, are omitted in the block diagram and in the design as well.

5.2 Design of an Inductor-Capacitor-Based Voltage Controlled Oscillator

The VCO is an integral part of today’s high speed or RF communication circuits. Transmitters and receivers both require high-performance VCOs. Ring-oscillator and relaxation-type VCOs are limited in their ability to support
narrowband applications with high output levels at low cost, whereas inductor-capacitor-based VCOs (LC-VCOs) can provide good performance at the low costs required by many applications. In particular, LC-VCOs have lower phase noise than ring-oscillator VCOs, making it a necessary design choice when good phase-noise performance close to the carrier is required.

An LC-VCO is an oscillator where the principal variable or tuning element is a varactor capacitor. The VCO is tuned across its band by a DC voltage, $V_{tune}$, applied to the varactor to vary the net capacitance applied to the tuned circuit. An LC-VCO typically consists of an LC tank and a circuit that generates a negative conductance for compensating the losses in the LC tank. The LC-VCO core circuit is based on a cross-coupled MOS transistor pair, which creates the effective negative conductance. The following equation has to be fulfilled to achieve oscillation start-up conditions.

$$- G_m > \frac{1}{R_P}$$  \hspace{1cm} (5–1)

where $G_m$ is the negative conductance, and $R_p$ is the equivalent parallel resistance of the LC tank.
5.2.1 Small Signal Model of a CMOS VCO

The topology of the designed LC-VCO for the direct conversion transmitter is shown in Figure 5–3. It uses on-chip inductors ($L_1$ and $L_2$) and varactors ($C_{V1}$ and $C_{V2}$). The load usually is the input of CMOS buffers and hence capacitive. Figure 5–4 is drawn based on the equivalent circuit model of an CMOS oscillator in [28], where the broken line in the middle represents either the common mode or ground. The symmetric planar spiral inductor model of Figure 5–5 with identical RC loading on both terminals is used as a part of the tank model. The parasitic capacitance of inductors is represented by $C_L$, which is equal to $C_s + C_p$. $R_s$ is the parasitic resistance in series with inductance $L$. $R_p$ represents the shunt resistance...
Figure 5–4. Equivalent circuit model of the designed CMOS LC-VCO across the port and ground. The quality factor \((Q_L)\) of the L-R series combination is then given by \(Q_L = (\omega L)/R_s\), where \(\omega\) is the operation frequency.

Varactors are modeled with a capacitor \(C_V\) in series with a resistor \(R_V\).

The parasitic capacitances from a MOS transistor are described as \(C_{MOS}\), which includes \(C_{db}, C_{gs}, C_{gb}\) and \(C_{gd}\). The series resistance \(R_{MOS}\) mainly comes from the substrate resistances associated with source or drain to substrate junction capacitor \((C_{db} \text{ or } C_{sb})\) and gate to substrate junction capacitor \((C_{gb})\) [29]. The quality factor for a capacitor, \(Q_C\), is given as \(1/(\omega RC)\), where \(\omega\) is the operation frequency, \(R\) is the parasitic resistance in series with capacitance \(C\). Therefore, large contact
arrays are necessary to lower $R_{MOS}$ to improve the quality factor of $C_{MOS}$. $g_m$ and $g_o$ are small-signal transconductance and output conductance of the transistors, respectively.

5.2.2 Noise Issue Considerations

The noise of the free-running VCO is a dominant noise contributor in an RF communication circuit. In that respect, MOS LC-VCOs especially represent a challenge for RF circuit design because of the high $1/f$ noise in the CMOS process. Moreover, the scaling of CMOS technology leads to lower supply voltage and hence lower VCO tank voltage swing, which could degrade the VCO’s phase noise performance. Close-in phase noise is a major drawback for CMOS VCOs because of the high $1/f$ noise of the MOS transistors. A great deal of the close-in noise comes from the up conversion of the $1/f$ noise through the tail transistor. Compared to NMOS transistors, PMOS transistors contribute less thermal noise and $1/f$
noise. Moreover, since the $1/f$ noise is inversely proportional to a transistor’s gate area, a PMOS transistor, M3, with large width and length (450 µm/500 nm) is therefore used as the tail transistor to reduce the close-in phase noise. Meanwhile, since PMOS transistor’s overdrive voltage is low thanks to its large width, it leads to a smaller voltage drop across the transistor’s source and drain when the transistor is working in saturation. This adds to the advantages of using a PMOS transistor for the tail current source in that it can leave more headroom for the VCO’s output voltage swing, which also helps improve phase noise performance [30]. However, it should be pointed out that, because NMOS transistors have smaller size than PMOS transistors to achieve the same $G_m$, cross-coupled NMOS transistors (M1 and M2) are used for the negative conductance generation part of the CMOS LC-VCO circuit, in order to achieve a larger tuning range than its PMOS counterpart.

For LC-VCOs, the overall Q of the LC tank is also a key factor that determines the phase noise performance. Normally, the Q factor of the LC tank is determined by the inductor. A differential spiral inductor with a polysilicon patterned-ground shield (PGS) is used in this VCO design to achieve a higher Q. This is also a good match to the differential VCO topology. A large value of the inductance $L$, or a small $C/L$ ratio, can relax the requirement for the value of $G_m$, and hence reduce power consumption [31]. In this work, the value of $L$ is designed to be 880 pH for the oscillating frequency of 5 GHz. Varactors are implemented with MOS capacitors. A MOS transistor with its drain, source, and bulk (D, S, B) connected together can realize a MOS capacitor, and the value of the capacitance
Figure 5–6. Layout of the LC-VCO circuit
is dependent on the voltage between bulk (B) and gate (G), $V_{BG}$. MOS varactors have an approximately similar tuning range and better phase noise performance than diode varactors [32]. The value for the varactors was targeted at 800 fF for an oscillating frequency of 5 GHz with an estimated tuning range from 492 fF to 1.056 pF. A varactor’s tunability is defined to be $C_{max}/C_{min}$. Therefore, the estimated tunability of the varactor is 2.15.

The layout of the LC-VCO circuit is shown in Figure 5–6. The VCO is designed to oscillate at around 5 GHz, which is twice the desired LO frequency. The output of the VCO will be connected to a 2:1 frequency divider, which was introduced previously as one of the circuit blocks for the modulator, to generate four LO signals with phases in quadrature with one another. The simulation result of the generated quadrature LO signals can be seen in Figure 5–7.

5.3 Design of a Power Amplifier

5.3.1 Basic Characteristics of a Power Amplifier

RF/Microwave power amplifiers are an important circuit component used in almost every communication system including cordless and cellular telephone, base station equipment, satellite communications, wireless LANs, and so on. However, they remain a challenging building block in RF circuit designs. Some of the important characteristics of an amplifier include linearity, efficiency, and output power. Usually there are tradeoffs between these characteristics. For example, improving amplifier’s linearity will degrade its efficiency. A linear
Figure 5–7. Simulated result of the output of VCO plus divider amplifier preserves the details of the signal waveform, that is to say, \( V_o(t) = A \cdot V_i(t) \) (5–2)

where, \( V_i \) and \( V_o \) are the input and output signals respectively, and \( A \) is a constant gain. But if \( V_i \) contains higher power, then the amplifier could produce nonlinear distortion.

The drain efficiency of a power amplifier (PA) is a measure of the amplifier’s ability to convert the dc power of the supply into the signal power delivered to the load. The definition of drain efficiency is as follows: \[ \eta = \frac{\text{signal power delivered to load}}{\text{DC power}}. \]
If an ideal amplifier exists, the power delivered to the load would equal the power taken from the DC supply. In reality, an amplifier efficiency of one is not possible, especially in RF circuits. In many high frequency systems, the output stage and driver stage of an amplifier consume power in the amplification process. However, some power amplifiers provide higher efficiency than others. What kind of power amplifier should be designed depends on the application requirements. Generally speaking, linear modulations employ amplitude change to carry the data information, and hence can only allow for linear but not-so-efficient power amplifiers. However, for constant envelope modulations, power efficient non-linear amplifiers is an appealing candidate because signal distortion will not be a concern.

5.3.2 Classes of Power Amplifiers

Depending on the relation between the input and output signals, circuit configurations, and modes of operation, power amplifier circuits can be classified into different classes. RF/microwave power amplifiers are generally defined to operate in class A, B, AB, C, D, E, and F. These classes are implemented by selecting bias conditions of the active device and by designing input and output match, to meet system requirements in terms of output power, efficiency (or DC power consumption), linearity conditions (modulation schemes), frequency range, size, weight, and cost [34].

However, a trade-off between the efficiency and linearity exists for PAs of any class. That is, higher efficiency means poorer linearity and vice versa. For example, let us compare class A, B, and C PAs to see the trade-off. Among the three, the
class-A amplifier has the highest linearity. The amplifier operates in the device’s linear region and is conducting current constantly, which means more power loss and lower power efficiency. An ideal class-B amplifier operates at zero quiescent current, because the output current is off for half of an input sinusoidal signal cycle. This lowers the power consumption and improves the efficiency, but the linearity of the device is degraded. In applications where linearity is not a concern, a class-C amplifier can be a good choice. A class-C amplifier is biased such that the output current is zero for more than half of the input signal cycle. Therefore, its efficiency will be even higher than a class-B amplifier. The theoretical values for the highest possible efficiency of class A, B, and C amplifiers are 50%, 78%, and 100%, respectively. In practice, however, an efficiency of 100% is improbable because the current cannot be switched off completely.

The different classes are further discussed below.

**Class A.** The active Device in a class A PA is conducting at all times. In other words, there is current for the full cycle (360°) of an input sinusoidal signal. The quiescent point, Q, is set to approximately the center of the device current, as can be seen in Figure 5–8 [34], where $I_p$ and $V_{DD}$ are the peak current and
drain supply voltage, respectively. The linear output power can be maximized by proper load matching. Designing a class A PA is, in a sense, the same as designing a small-signal linear amplifier because the output signal is expected to duplicatively amplify the input signal. But a class A PA operates at higher power level than small-signal amplifiers. We know that more output power can be obtained when an amplifier works in the saturation mode. However, the harmonics and distortion will be less severe if the amplifier is not operated far into saturation. With the active device working in the linear region, a class A amplifier provides the highest linearity and almost exactly the same output waveform as the input signal, although its maximum drain efficiency is limited to 50%.

**Class B.** The Q point in class B is at the cutoff of the device current (Figure 5–8) and the active device conducts only one half of a cycle (180°) of the input sinusoidal signal. Instead of obtaining maximum linear output power as in the case of class A, the load in class B is matched to achieve best gain and maximum efficiency possible. Class B RF amplifiers often adopt a push-pull configuration, which has two single-ended stages that share the output load. In a push-pull configuration, one amplifier stage only operates during the positive cycle of the sinusoidal wave when the transistor pushes current into the load, and the other stage only the negative cycle when the transistor pulls the current from the load. The linearity performance of single-ended class B amplifiers is not as good as class A. However, they have higher efficiency because each device is turned on for only
half a cycle of the input signal. The maximum drain efficiency of class B amplifiers is 78%.

**Class C.** If the Q point is well below the cutoff point of the device current and hence the device only conducts 25-45% of a sinusoidal cycle of the input signal, then the power amplifier is operating in class C, where only some portion of the positive cycle of the sine wave is amplified. Class C amplifiers are very nonlinear and the output waveform is quite different from the input signal. But they have higher efficiency than both class A and class B amplifiers because the active device is turned on for even less than half a period during each sinusoidal cycle. Class C amplifiers are often used when the modulation scheme does not require device linearity.

**Class D or E.** In class D or E PAs, the active device works in two states, “ON” and “OFF”, like a switch. In the “ON” state, the device resistance is very low or negligible, and there is no power dissipation. In the “OFF” state, the device’s impedance is very high, and no current flows through it. Therefore, an ideal class D or E amplifier can achieve 100% drain efficiency. However, the efficiency is always reduced in practice because of the device’s finite “ON” resistance and the transition time between the two states. It should be noted that a class E amplifier is different from a class D one in that it has a tuned circuit at the output to provide the desired reactive load at the fundamental frequency.

**Class F.** A class F PA is similar to the class D or E PAs in the sense that the device also works as a switch and the theoretical efficiency is 100%. It uses
impedance matching at the output to terminate harmonic frequencies, in order to reduce power dissipation. Ideally, the output circuit of a class F amplifier should be designed to present a short circuit to the second harmonic and an open circuit to the third harmonic. However, due to the difficulty in designing matching circuits over a large bandwidth, oftentimes only the short at the second harmonic is aimed at in practice.

5.3.3 Design of a Nonlinear Power Amplifier for the Output of the Constant Envelope Modulator Circuit

Constant envelope modulations, such as MSK and GMSK, allow the power amplifier (PA) to be operated in saturation, and can achieve greater efficiency than linear modulations. The modulator introduced in the previous chapter can generate a constant envelope modulated signal, and therefore can be used in a low power transmitter utilizing a non-linear PA, such as a Class B or a Class C PA.
Figure 5–10. Buffers to drive the PA. (a) Buffer for the first three stages (b) Buffer for the last stage
Figure 5–11. Layout of the PA and its proceeding buffer/driver
Figure 5–12. Simulated differential output waveform from the PA

Single-ended class A, B, and C amplifiers have the same topology (Figure 5–9), and are differentiated by their bias conditions. The power amplifier designed in this work is biased between single-ended class B and class C configurations. It is not exactly a class C amplifier because the bias condition borders on that for a class B amplifier, although the gate voltage is still lower than the device’s threshold voltage. The bias condition has to be set in such a way that the output signal level is acceptable. The configuration of the designed power amplifier is the same as the one shown in Figure 5–9. Biasing is done at the Vbias node, and Ccpl is a coupling capacitor to AC-couple the signal from the previous stage of the circuit and feed it into the power amplifier gate together with the bias DC voltage. Note that a tuned circuit at $f_0$ or a filter is necessary for a class C amplifier to reduce the signal distortion caused by the high non-linearity of the amplifier.
In this design, there are a series of buffers, as also shown in Figure 5–10, between the output of the modulator and the input of the power amplifier, in order to drive the signal level high enough for the amplifier to saturate. The buffer topology for the first three stages is similar to that used in the modulator design, and the last stage used two single ended buffers with inductor loads instead of resistors to further boost up the signal swing before sending it into the PA. The layout of the PA and its proceeding buffer/driver is shown in Figure 5–11.

Simulation of the whole transmitter chain showed a result of the PA’s output waveform, as can be seen in Figure 5–12. The simulation was done by applying the same gate bias voltage, which is a little lower than the threshold voltage of both devices, to the PA and its proceeding driver. The reason for biasing the driver this way is to reduce its power consumption.

5.4 Experimental Result of the Direct Conversion Transmitter Circuit

The designed LC-VCO, the modulator for arbitrary data patterns, and the PA are put together to form a simple direct conversion transmitter circuit. The circuit was fabricated in a 0.18 µm mixed signal CMOS process. The die microphotograph of the circuit is shown in Figure 5–13. The area of the chip is 1.094 mm².

The transmitter circuit was tested in a similar way to the testing of the modulator circuit, as can be seen in Figure 5–14 for the measurement setup. The signal generator that was used for testing the modulator circuit is not needed, because the RF signal, which is at a frequency twice the desired carrier frequency, can be generated by the on-chip LC-VCO circuit. The supply voltage, bias
voltages, and control voltage \((V_{\text{tune}})\) for the LC-VCO are provided by batteries in order for a more steady VCO output.

There are no stand-alone testing circuits for two of the building blocks of the transmitter circuit, the LC-VCO, and the PA with its drivers. The LC-VCO and the PA are the preceding and succeeding blocks, respectively, of the modulator circuit which has been tested and introduced in the previous chapter. However, each block is controlled by separate supply voltages and biases, and therefore the three blocks can be turned on sequentially to allow us to see the signals they generate from the spectrum analyzer, which is connected through an RF probe.
Figure 5–14. Measurement setup for testing the transmitter circuit to the on-chip output signal pads. It should be noted that, when the PA is not turned on, the signals which can be observed on the spectrum analyzer, from either the LC-VCO alone or the LC-VCO plus the modulator, are coupled to the output signal pads through the substrate, because there are no real signal paths from the LC-VCO or the modulator to the pads. Figure 5–15 shows the substrate-coupled output of the LC-VCO and the modulator’s 2:1 divider (with no data or clock applied to the modulator).

The tuning range of a VCO can be defined as

\[
\text{tuning range} = \frac{f_{\text{max}} - f_{\text{min}}}{(f_{\text{max}} + f_{\text{min}})/2}
\]  \hspace{1cm} (5–4)

With a tuning voltage between -1 V and 2.8 V, the measured tuning range of the LC-VCO through substrate coupling is from 4.5 GHz to 6.3 GHz. Therefore,
we can roughly estimate the tuning range of the LC-VCO to be 33.3% or larger, which is a little better than the 10-30% typical tuning range for CMOS LC-VCOs [29]. Since the oscillating frequency of an LC-VCO is inversely proportional to the square root of the capacitor value of the LC tank, the measured operating frequency range of the LC-VCO incurs a tunability of 1.96 for the varactor used in the LC-VCO design, which is slightly lower than the estimated value when designing the LC-VCO. But considering that the measured frequency range is obtained based on the signal detected through substrate coupling, this tunability value is in line with the simulation result.

With the LC-VCO tuned at around 5 GHz, the carrier frequency is 2.5 GHz for the modulator and the entire transmitter. Applying data and clock at different
Figure 5–16. Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 12 Mbps bit rate

rates to the modulator, and biasing the PA at a gate-to-source voltage slightly higher than the device’s threshold voltage, the transmitter circuit’s output signal spectra at different data rates can be observed and recorded from the spectrum analyzer. Figures 5–16, 5–17, 5–18, 5–19, and 5–20 show the power spectra of the output signal at 12 Mbps, 25 Mbps, 37.5 Mbps, 50 Mbps, and 100 Mbps bit rate, respectively.

The calibrated output signal power level of the transmitter circuit at 2.5 GHz carrier frequency is around 3 dBm. The current dissipations of the LC-VCO, the modulator, and the PA with its drivers are 11 mA, 2 mA, and 59 mA respectively. The supply voltages for the composing blocks are all 1.8 V. Therefore, the power consumption of the entire transmitter circuit is 129.6 mW. The transmitter’s output RF power level within the frequency range of 2.3 GHz to 3 GHz is
Figure 5–17. Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 25 Mbps bit rate

Figure 5–18. Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 37.5 Mbps bit rate
Figure 5–19. Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 50 Mbps bit rate

Figure 5–20. Measured power spectrum of the transmitter circuit at 2.5 GHz carrier frequency and 100 Mbps bit rate
Figure 5–21. Output RF power level of the transmitter circuit vs. carrier frequency plotted in Figure 5–21. The drain efficiency of the PA is not high, although a high efficiency nonlinear PA would suit the circuit very well thanks to the constant envelope modulator output. The probable reasons for PA’s low efficiency include high bias voltage applied at the gate of both the PA and its drivers to boost up the signal level, the under-estimated parasitics of the circuit, and the over-estimated output signal power level from the VCO and the modulator. Although the PA design is not optimized, it serves the purpose of amplifying the modulator’s output signal level and preserving the spectrum. More importantly, we have successfully demonstrated that the modulator can be easily integrated into a transmitter system and works fine.

Table 5–2 briefly summarizes the performance of the direct conversion transmitter circuit.
Table 5–1. Performance summary of the direct conversion transmitter

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18 μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size</td>
<td>1.094 mm²</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.5 GHz</td>
</tr>
<tr>
<td>Modulation</td>
<td>MSK-like</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Current dissipation</td>
<td>72 mA</td>
</tr>
<tr>
<td>Output power</td>
<td>0 dBm</td>
</tr>
</tbody>
</table>

It should be pointed out that, unlike the measurement of the modulator circuit, the transmitter output’s constellation and I/Q diagram were not tested. The reason is that the phase of a free-running VCO is not fixed but rather constantly changing. Hence, the correctness of the four LO signals’s phase cannot be guaranteed. Therefore a clean and nice signal constellation is very unlikely. However, as we have shown in the previous chapters, if the output of the LC-VCO is replaced by the signal generated by a synthesizer, the modulator circuit is able to produce fairly accurately modulated signals. Moreover, because of the constant envelope feature of the modulator’s output signal, the power amplifier will not degrade the modulation, which is embodied in the signal’s phase rather than its amplitude. Therefore, we believe that the transmitter can produce an amplified signal with good modulation accuracy when the phase of the free-running LC-VCO is locked, which is in practice oftentimes the case with applications transceivers.

5.5 Direct Conversion Transmitter using a Quadrature Voltage Controlled Oscillator

A slightly different direct conversion transmitters was also designed and fabricated in a 0.18 μm CMOS process. The basic architectures for both of the
Figure 5–22. Direct conversion transmitter to be designed

designed transmitters are the same as the one shown in the block diagram in
Figure 5–22. The difference lies in the quadrature LO generating circuit.

Two commonly used methods to generate quadrature LO signals from voltage
controlled oscillators are VCO plus a frequency divider and quadrature VCO.
Comparative study has shown that the topology of a VCO plus a divider performs
better in terms of phase noise [35], and is better at mitigating the problem of LO
pulling in a direct conversion transmitter [36]. The first transmitter which was
introduced earlier in this chapter used this method, i.e., a VCO at twice the desired
LO frequency plus a 2:1 frequency divider.

Another topology for generating quadrature LO signals is a quadrature VCO
(QVCO) circuit. This method relies on direct quadrature generation at the output
of the QVCO, which operates at the desired frequency without other accompanying
circuit components. The second transmitter used this method. We will now
introduce the design of the QVCO first, and then present the experimental results
of the direct conversion transmitter using the QVCO circuit.

5.5.1 Design of a Quadrature Voltage Controlled Oscillator

A QVCO can be obtained by cross-coupling two identical oscillator cores,
resulting in a configuration as shown in Figure 5–23. VCO2 is connected to VCO1
in anti-phase, while VCO1 is connected to VCO2 in common phase. This yields a 180-degree delay in phase from VCO2’s output to VCO1’s input, forcing the two VCOs to synchronize such that the phase delay in each is exactly 90 degrees, assuming they are identical. Each oscillator core has been designed as a basic fully differential LC-VCO, and the overall circuit topology for the QVCO can be seen in Figure 5–24.

The QVCO is based on the cross-coupling of two differential LC-VCOs. In each LC-VCO core, the coupling transistors (M3 and M4) are placed in parallel with the switch transistors (M1 and M2). In such QVCOs, both phase noise and
Figure 5–25. Layout of the LC-QVCO
phase error are strong functions of \( \alpha \), defined as the ratio of the width of the coupling transistors to the width of the switch transistors [37]. Study has shown that the phase error gets quickly larger when the coupling between the two VCOs is weakened by decreasing \( \alpha \). On the other hand, the phase noise greatly decreases with a decreasing \( \alpha \) [37]. Therefore, improving the phase noise performance of a QVCO will be at the expense of the QVCO’s phase error performance. In this QVCO design, phase error is also a critical factor which can affect the modulator’s accuracy. Besides, simulations have shown that the QVCO’s output voltage swing is the biggest when \( \alpha \) equals 1/2. With all this taken into account, the widths of the coupling transistors and switch transistors are designed to be 108 \( \mu m \) and 216 \( \mu m \), respectively.

The QVCO was designed to oscillate at around 2.5 GHz. Accordingly, the value of the inductors was chosen to be 3 nH, and the varactors were designed to be 1.1 pF with an estimated tuning range from 677 fF to 1.452 pF. The layout of the LC-QVCO is shown in Figure 5–25. The simulation result of the generated quadrature LO signals can be seen in Figure 5–26. The block diagram of the direct conversion transmitter utilizing such a quadrature LO generation circuit topology is shown in Figure 5–27. It can be seen that the architecture of the two transmitters are almost the same except for that a QVCO replaced the VCO plus divider topology in the second transmitter.
Figure 5–26. Simulated result of the quadrature LO signals generated by the QVCO

Figure 5–27. Block diagram of the direct conversion transmitter utilizing an LC-QVCO
5.5.2 Experimental Result of the Transmitter Circuit using QVCO

Figure 5–28 shows the die microphotograph of the transmitter circuit using a QVCO. The area of the chip is 1.256 mm$^2$. The measurement setup is almost the same as illustrated in Figure 5–14.

With a tuning voltage between -1 V and 2.8 V, the measured frequency range of the QVCO through substrate coupling is from 2.33 GHz to 3.1 GHz. Therefore, we can roughly estimate the tuning range of the LC-VCO to be 28.36% or larger, which is within the 10-30% typical tuning range for CMOS LC-VCOs [29]. The measured operating frequency range of the LC-VCO incurs a 1.77 or higher tunability for the varactor used in the LC-VCO design.
The calibrated output signal power level of the transmitter circuit at 2.6 GHz carrier frequency is 1 dBm. The current dissipation at the LC-QVCO, the modulator, and the PA with its drivers are 10 mA, 2 mA, and 58 mA respectively. The supply voltages for the composing blocks are all 1.8 V. Therefore, the power consumption of the entire transmitter circuit is 126 mW.

Figures 5–29, 5–30, and 5–31 show the power spectra of the output signal at 12 Mbps, 25 Mbps, and 37.5 Mbps bit rate, respectively. It can be seen that the direct conversion transmitter using a QVCO has a LO leakage problem which is quite obvious at a data rate of 37.5 Mbps or higher. This is probably because the operating frequency of the QVCO and that of the PA are in the same range, which is one of the drawbacks of such direct conversion transmitters. The previously introduced transmitter circuit uses a VCO which operates at twice the carrier frequency, and hence it can alleviate the LO disturbance caused by the PA to some extent.

Table 5–2 briefly summarizes the performance of the direct conversion transmitter circuit using a QVCO.

<table>
<thead>
<tr>
<th>Table 5–2. Performance summary of the direct conversion transmitter using a QVCO</th>
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<tbody>
<tr>
<td><strong>Technology</strong></td>
</tr>
<tr>
<td><strong>Die size</strong></td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
</tr>
<tr>
<td><strong>Modulation</strong></td>
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<tr>
<td><strong>Power supply voltage</strong></td>
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<tr>
<td><strong>Current dissipation</strong></td>
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<tr>
<td><strong>Output power</strong></td>
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Figure 5–29. Measured power spectrum of the transmitter circuit using a QVCO at 2.56 GHz carrier frequency and 12 Mbps bit rate

Figure 5–30. Measured power spectrum of the transmitter circuit using a QVCO at 2.56 GHz carrier frequency and 25 Mbps bit rate
The digitally controlled phase shift modulator can be easily integrated into both transmitter systems. Compared to the transmitter utilizing a QVCO to generate the four quadrature LO signals the modulator needs, the topology of a VCO plus a frequency divider proves to mitigate the LO leakage problem. But in either system, the modulator circuit functions well and requires no baseband processing for data.
In the previous chapters, we demonstrated the constant envelope modulation function of the modulator circuit, and its suitability for a ZigBee radio compliant with the IEEE 802.15.4 standard. We also presented that the modulator can easily be integrated into a simple direct conversion transmitter, which could be a good choice for personal area networks. However, whether in a stand-alone test chip or integrated in a direct conversion transmitter, the modulator circuit is designed to realize an MSK-like modulation only. Now we address the software reconfigurability of the modulator. Thanks to the phasor combining approach and the circuit topology designed based on this approach, a modulator circuit core, which can be controlled by peripheral signals on a circuit board, can be similarly designed in an effort to generate some different modulation schemes. The goal of building a software configurable board-level modulator is to roughly demonstrate the applicability of the proposed modulator for a software defined radio.

6.1 Design of the Modulator Circuit Board

The integrated modulator circuit which was described in previous chapters works specifically for an MSK-like modulation, but the design was based on the phasor combining approach which is expected to be applicable for some of the other modulation schemes as well. Figure 6-1 retells the principle of the approach, which simply says different phases ($\theta$) and/or amplitudes of $V_{\text{out}}$ can be generated from
two phasors (V1 and V2) in quadrature by applying different summing weights (a and b).

Recall that, among the building blocks of the modulator circuit (Figure 4–4), the two 4:1 multiplexers select and provide two phasors in quadrature in the correct quadrant, and the summing circuit (Figure 2–4) uses the two bias currents (I1 and I2) to weigh V1 and V2 respectively in order to produce the desired output phasor (Vout). Therefore, the implementation of software control over the output phasor according to the desired modulation takes place with the bias current sources for the summing circuit.

In the original IC design for the MSK-like modulator, four phasors (P0, P1, P2, and P3) need to be generated within each bit interval, or each quadrant on the I/Q plane. It was realized by digitally generating four different combinations of current sources as four different sets of weights for V1 and V2. As can be seen from Figure 6–2, digital control signals are applied to the three switches repeatedly.
over the bit intervals. Each bit interval is divided into four subintervals ($t0$, $t1$, $t2$, and $t3$), each for one phasor (P0, P1, P2, and P3, respectively). The two bias currents ($I1$ and $I2$) for the summing circuit take on different values during the four subintervals, thanks to the switches turning on or off the current sources ($I_{b1}$, $I_{b2}$, and $I_{b3}$), and hence generate the four different phasors in $V_{out}$.

Figure 6–3. Constellation of an OQPSK signal
As introduced earlier, the MSK modulation scheme can be regarded as the derivation of OQPSK, in that the square pulse shape in OQPSK is replaced by the half sine pulse shape in MSK. The square pulse shape in OQPSK results in non-continuous phase shift within each bit interval. As a matter of fact, the phase of the modulated signal remains constant for one bit interval, and it could either remain constant or jump by 90° for the next bit interval, depending on the data combination of the two channels for the next bit interval. Thus, the constellation of an OQPSK signal shows four signal points, one in each quadrant and 90° apart from one another in phase. The constellation and its symbols for an OQPSK signal is shown in Figure 6–3.

![Diagram](image)

Figure 6–4. Illustration of how the correct quadrants can be selected by the multiplexers for OQPSK

It is straightforward to implement the OQPSK modulation scheme using the same architecture as the MSK-like modulator. The modification will mainly take place with the bias currents for the summing circuits to implement software
control. More specifically, instead of four discrete phasors per quadrant, only one phasor needs to be generated for each bit interval. Therefore, the values of the summing circuit’s bias currents I1 and I2 can be fixed and equal at all times. Thus, as long as the correct quadrant is selected by the two multiplexers, the resulting output signal will be the desired phasor in the quadrant. Figure 6–4 explains how the multiplexers can guarantee that the correct quadrants be selected according to the data bits. It can be seen that, for each bit interval, the two outputs from the multiplexers are two phasors in quadrature constituting the correct quadrant on the constellation. It should be noted that the parallel 2-bit data symbols in parenthesis are only incurred by the 90° bit stream offset on the I channel (without loss of generality), they do not contain real data information.

Based on these considerations, a modulator chip to be used as the core circuit on the circuit board was designed and fabricated in the TSMC 0.18 μm CMOS
Die microphotograph of the modulator core circuit process. The design basically consists of the two 4:1 multiplexers, the summing circuit, and some digital control circuit for data and clocks. However, the summing circuit’s bias currents will be provided by current sources built on circuit board, because it will make it easier to change the currents and hence the output phasor. The block diagram and the die photo of the modulator core circuit is shown in Figure 6–5 and Figure 6–6, respectively.

As can be seen from the die photo, besides the DC supplies and biases, the core circuit needs four quadrature LO input signals at around 2.5 GHz, from which the two 4:1 on-chip Multiplexers will select the correct pair of quadrature phasors V1 and V2. It also needs clock and data input to perform modulation. The two pads labeled I1 and I2 are what the off-chip control currents for the summing circuit will flow through. The differential output signal will be the generated output phasor (Vout).

The printed circuit (PC) board was designed based on the specifications of the FR4 board provided by Advanced Circuits. Specifically, \( \epsilon_r = 4.5 \), \( TanD = 0.018 \).
(at around 2 GHz), $H = 62$ mil ($\approx 1.6$ mm), and $T = 2.1$ mil ($\approx 0.053$ mm). The input signals that the core circuit needs include the four quadrature LO signals at the frequency of around 2.4 GHz, and data and clock feed-ins at up to several hundred megahertz. The differential output signal will be at the same frequency as the LO signals. Therefore, transmission lines are needed for the transmission of these input and output signals. Using Linecalc in ADS (Figure 6–7), the width of the microstrip transmission line was calculated to be around 2.9 mm based on the specifications of the FR4 board. As for the DC supply and bias voltages, on-board bypass capacitors need to be shunted between them and ground.

The PC board was designed using Protel. It is a two-layer board (top and bottom) with vias. the layout of the board is shown in Figure 6–8.
Figure 6–8. Layout of the printed circuit board designed in Protel

Figure 6–9 shows the bonding diagram of the circuit. Ball bonding was performed to wire bond the core circuit chip to the board. Because the top layer metal is copper, which can easily oxidize, bonding was done by placing gold bond balls on top of each bond pads on the board while the copper has not oxidized yet. Thus, the balls have a better chance to stick on the pads. Then, gold bond wires can be placed to connect the aluminum pads on the core circuit chip and the gold balls on the bond pads of the board. Figure 6–10 shows what the bonded chip looks like on the board.

### 6.2 Experimental Results

The picture of the completed modulator circuit board is shown in Figure 6–11. The dimension of the board is 2.58 inch by 2.36 inch.

Figure 6–12 shows the measurement setup for testing the modulator board. The signal generator provides an AC signal at the desired carrier frequency, or LO frequency for the modulator. The 90° balun and the pair of 180° baluns are
Figure 6–9. Bonding diagram for the core circuit chip

Figure 6–10. Photo of the bonded chip on the PC board

Figure 6–11. Photo of the completed PC board
Figure 6–12. Measurement setup for testing the modulator board

Figure 6–13. Schematic of the board-level current source

Figure 6–14. Photo of the current source test board for OQPSK modulation
connected to generate four LO signals in quadrature with one another. These four signals are fed into the modulator circuit though the four LO inputs. Agilent N4906A bit error rate tester (BERT) is used to provide the circuit with data and clock inputs. The modulator’s differential output signal is measured by terminating one end with 50 Ω and connecting the other end to a spectrum analyzer.

The external control current sources are built on a bread board using discrete transistor parts. Because the board-level modulator maintains the same circuit architecture as the integrated modulator circuit, emphasis was placed on generating OQPSK modulation in testing the board, because the MSK modulation function of the circuit has been demonstrated earlier on. For OQPSK, only two current sources with equal current values are needed to bias the summing circuit. KN2222/A epitaxial planar NPN transistors and 100 kΩ potentiometers were used to build the current sources. The schematic of a current source is shown in Figure 6–13, and the photo of the current source test boards is shown in Figure 6–14.

The theoretical power spectrum of an OQPSK signal is plotted in Figure 6–15. The measured output spectra showed very consistent results, as can be seen from Figure 6–16.

Figures 6–17, 6–18, and 6–19 show the measured output spectra at the carrier frequency of 0.5 GHz, 1 GHz, and 3 GHz, respectively, with a data rate of 24 Mbps (minimum data rate available from the BERT). Figures 6–20, 6–21, and 6–22 are the measurement results when the carrier frequency was set to 2.4 GHz, while the data rate was 40 Mbps, 80 Mbps, and 100 Mbps, respectively. The resolution bandwidth of the spectrum analyzer was set to 3 MHz for all the measurement
Figure 6–15. Theoretical power spectrum of OQPSK

Figure 6–16. Consistent measurement result with theoretical spectrum

results. For generating OQPSK, the current dissipation of the whole modulator circuit board is 15 mA, and the supply voltage is 1.8 V.

The modulator board uses a core circuit that has the same architecture except that the on-chip implementation of software control over the current sources, which was introduced in the previous section, was removed from the core circuit. The exact same circuitry can be built on board using discrete transistor parts, and even more phasors per quadrant, e.g., 8 or 16, can be possibly created by
Figure 6–17. Measured output spectrum at 0.5 GHz carrier frequency and 24 Mbps data rate

Figure 6–18. Measured output spectrum at 3 GHz carrier frequency and 24 Mbps data rate
Figure 6–19. Measured output spectrum at 3.7 GHz carrier frequency and 24 Mbps data rate

Figure 6–20. Measured output spectrum at 2.4 GHz carrier frequency and 40 Mbps data rate

Figure 6–21. Measured output spectrum at 2.4 GHz carrier frequency and 80 Mbps data rate
Figure 6–22. Measured output spectrum at 2.4 GHz carrier frequency and 100 Mbps data rate

Figure 6–23. Comparison of the power spectra for different number of phasors per quadrant
generating more combinations of bias current sources. The more phasors there are per quadrant, the closer the output spectrum will be to the theoretical power spectrum of MSK (Figure 6–23). Because the MSK modulation function has been demonstrated by the integrated circuit presented earlier, it is reasonable to infer that the modulator circuit board is capable of generating MSK modulation as well. Hence, the modulator circuit board can be used to demonstrate the software reconfigurability of the modulator.
CHAPTER 7
SUMMARY AND FUTURE WORK

7.1 Summary

A modulator that has the potential to generate different modulation schemes is proposed and presented. The modulator uses a “digital” approach rather than the conventional analog modulators using the “mixing” or “multiplying” approach. The digital approach uses the phasor combining technique to generate the modulated signal constellation, which is essentially to weigh and sum up two phasors, or two LO signals with different phases, e.g, in quadrature, so that a desired phasor which represents the modulated signal on the constellation can be generated.

Two test modulator circuits realizing an MSK-like modulation scheme based on the phasor combining approach are designed and fabricated using the TSMC 0.18 μm mixed-mode CMOS technology, one with a fixed data pattern, the other for arbitrary data patterns. The experimental results show that, compared to conventional modulator of the similar functions, modulator circuits built using the phasor combining approach have the advantages of low power consumption, high data rate, broad operating frequency range, and less circuit complexity in terms of necessary accompanying circuit components for function and performance purposes. For example, the summing approach replaces signal mixing and hence relaxes the requirement for image rejection and harmonic filtering. Also, it reduces the burden of baseband processing on the digital circuit sector. Thus, if the modulator is to
be used in a software defined radio, in which it needs to be able to generate several
different modulation schemes, the baseband processing for the different schemes
can be greatly simplified. Another point worth mentioning is that, the modulator
circuit can become tailor-made for a ZigBee radio or some other device compliant
with IEEE 802.15.4, mainly thanks to its low power consumption and MSK
modulation function. It should be noted that, although only four discrete phasors
are generated for each bit interval while the ideal MSK modulation takes an infinite
number of them, the power spectrum can match the theoretical spectrum even
better simply by increasing the number of phasors per quadrant, as shown in
Figure 6–23 in the previous chapter.

The modulator circuit has less need for image rejection and filtering, and
hence a higher level of integrability. It can easily be integrated into a transmitter
chain, where the transmitter architecture can be either direct conversion or indirect
up conversion. As a matter of fact, the modulator design was employed in both
architectures as summarized in the following, and the testing results for both
transmitters proved the functionality and integrability of the modulator circuit.

The design of a direct conversion transmitter using the TSMC 0.18 µm
mixed-mode technology, which utilizes the modulator, and the experimental
results are presented as one of the applications of the modulator. Because the
modulator realizes a constant envelope phase shift modulation, it allows for the use
of a power-efficient nonlinear power amplifier in a transmitter, which makes the
transmitter a good choice for some low power wireless communication applications.
For example, the transmitter design introduced in the dissertation can be applied
for a ZigBee-ready personal area network, or some other similar wireless networks or sensor networks. It has the advantages of higher data rate and lower EVM than the normal specifications for such networks.

The modulator design was also applied to the \(\mu\)Node system development carried out by the SIMICS research group at the University of Florida. The \(\mu\)Node is a true single chip radio incorporating on-chip antennas, a transceiver, a digital baseband processor, a sensor, and potentially even a battery. It is being developed using standard CMOS technology and intended to be capable of wireless transmission and reception at \(\sim\)24 GHz over short distances. It can also be viewed as a modified ZigBee radio operated at 24 GHz. Figure 7–1 shows the simplified \(\mu\)Node RF subsystem block diagram, in which the highlighted block is the indirect up-conversion transmitter. The 24 GHz transmitter, which utilizes the constant envelope MSK-like modulator at the IF frequency of 2.7 GHz, was designed and fabricated in the UMC 0.13 \(\mu\)m Logic CMOS process. The measured output power spectrum at 100 Mbps data rate and I/Q plane constellation at 12 Mbps data rate are shown in Figure 7–2 [38].

In addition to its applicability for wireless communication transmitters, the modulator circuit’s reconfigurability was also addressed and demonstrated by the design and testing of a circuit board utilizing the core circuit of the modulator, which was fabricated in the TSMC 0.18 \(\mu\)m process. By slightly modifying the configuration of the bias currents for the summing circuit, an OQPSK modulation was implemented, which makes the modulator suitable for many more wireless communication applications where conventional I/Q modulators are normally used.
Figure 7–1. Simplified µNode RF subsystem block diagram

Figure 7–2. Measured output power spectrum (100 Mbps data rate) and constellation (12 Mbps data rate) around 24 GHz

EVM = 7.7% rms
In summary, the constant envelope phase shift modulator using the phasor combining approach has been demonstrated to work for an MSK-like modulation. It consumes very low power and has good modulation accuracy. Compared with conventional I/Q modulators, the proposed modulator has the advantages of relaxed requirements for image rejection and filtering, broader operating frequency range, and higher data rate. The modulator is most appealing and promising in that the concept behind it, which has been verified by experiment results, can be utilized to generate different modulation schemes. For example, GMSK modulation generates a signal whose phase change also follows a similar but more complicated pattern than MSK. Thus, it is possible to implement the phase change pattern of GMSK so that the conventional baseband circuit for Gaussian filtering or pulse shaping will no longer be required. Moreover, for any arbitrary modulations, only a finite number of steps between phase changes is needed, as long as the output power spectrum can meet the application-specific requirements. Therefore, as mentioned earlier, the modulator has a broad application prospect. It can be used in low power transmitters, especially those integrated with wireless sensors. It is also a good choice for a personal area network. More importantly, due to its digital control nature and potential for implementing different modulations such as QAM, the modulator would be well suited for a software configurable radio.

7.2 Future Work

The most immediate work that can be carried out is to modify the design of the modulator circuit board using the core circuit chip in the TSMC 0.18
μm technology. The purpose of the modification will be to build a single modulator circuit board that can generate and switch between OQPSK and MSK modulations. The OQPSK modulation function has been demonstrated in the previous chapter. The MSK function can be generated by building board-level current sources and digital control mechanism. More specifically, the two bias currents of the summing circuit, I1 and I2, are each provided by a series of current sources whose currents can contribute to I1 or I2 if the switches that are connected to them are turned on. The switches are turned on or off by peripheral digital control circuitry. Figure 7–3 conceptually illustrates how, in a 4 phasors per quadrant case, the correct values of I1 and I2 can be provided in order to generate a particular phasor. Without loss of generality, in this example, I_{P0} produces a weight that is proportional to \cos0^\circ, I_{P1} produces a weight proportional to \cos22.5^\circ, or \sin67.5^\circ, I_{P2} \cos45^\circ, and I_{P3} \cos67.5^\circ. Therefore, peripheral digital circuit needs to be built to realize this scheme, while synchronization to bit intervals is also a key consideration to be accommodated. Additional circuitry can be built to equip the modulator board with the ability of switching between the two modulation schemes with ease, for example, at the pressing of a button.

Based on this work, a new modulator test board for the purpose of generating more modulation schemes can be designed and built. The implementation of these modulations will utilize the same design principle but require different phase change patterns and different magnitude of the phasor as well for the case of QAM. A modulator core circuit chip for this purpose has been designed and fabricated using the UMC 90nm Logic CMOS process, and can be placed on the new test
Figure 7–3. How the correct values of I1 and I2 can be provided for a phasor board. Figure 7–4 shows the die photo of the core circuit chip. The architecture of the modulator core circuit is the same as previously introduced, and the main difference lies in that one-stage 4:1 multiplexers as published in [15] are used instead of the two-stage ones. The reason for using the one-stage 4:1 multiplexers is that it allows for easier selection of the correct quadrant which the modulated signal should falls in, according to the data bits.

Controls will mainly be applied over the clocking of the multiplexers and the generation of bias current combinations for the summing circuit. The multiplexers need to be clocked in order to select the correct quadrants on the constellation, and the phasor combining circuit will rely on its two bias/weighting current sources to produce the correct phase and/or amplitude on the signal constellation. It should be pointed out that, for this new core circuit, current sources and their switches are all integrated on the chip, but biasing the current sources and turning on/off
Figure 7–4. Die photo of the modulator core circuit using UMC 90 nm technology

the switches are still to be realized by DC voltages and control signals, respectively. Again, these controls are to be realized off chip by digital circuits or using high speed microprocessor applications. The resulting modulator circuit board will hopefully be able to accommodate different modulations such as QPSK/OQPSK, MSK, and QAM.
REFERENCES


BIOGRAPHICAL SKETCH

Xiuge Yang was born in Beijing, China. She received a Bachelor of Science degree in electronic engineering from Tsinghua University of China in 1999. She received a Master of Science degree in electrical and computer engineering and a Master of Science degree in management from the University of Florida in 2001 and 2003, respectively. In 2003, she joined the Radio Frequency System On Chip (RFSOC) Research Group, at the University of Florida Department of Electrical and Computer Engineering. Her research interests include RF and mixed signal integrated circuit design in CMOS technology, wireless communications, digital modulations, and software defined radio.