LOW-NOISE AND LOW-POWER INTERFACE CIRCUITS DESIGN FOR INTEGRATED CMOS-MEMS INERTIAL SENSORS

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2006
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by

Deyou Fang
To my parents;
to my wife, Tongsheng Li;
and to my son, Jim L. Fang.
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Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

LOW-NOISE AND LOW-POWER INTERFACE CIRCUITS DESIGN FOR INTEGRATED CMOS-MEMS INERTIAL SENSORS

By

Deyou Fang

May 2006

Chair:  Huikai Xie
Major Department:  Electrical and Computer Engineering

Deep reactive-ion-etch (DRIE) CMOS-MEMS technology has the potential to produce small-size, low-cost, high-resolution and low-power inertial sensors. In this work, design of CMOS electronics for integrated capacitive CMOS-MEMS inertial sensors is investigated. The goal of this investigation is to provide deeper understanding of low-power high-performance capacitive sensing circuits design and design trade-offs at three different levels: the theoretical, system and architecture, and transistor levels. The results of this work are used to obtain low-noise and low-power interface circuits integrated in monolithic CMOS-MEMS accelerometers and gyroscopes.

At the theoretical level, fundamental limits on power dissipation for CMOS capacitive sensing circuits regarding to other performance specifications are investigated. At the system and architecture level, optimization methods for minimum power consumption in chopper amplifier based continuous-time voltage sensing are provided. A novel dual-chopper amplifier (DCA) architecture is proposed to achieve both low-noise
and low-power dissipation simultaneously in capacitive CMOS-MEMS inertial sensors. In addition, an active mixer topology is proposed for replacing the conventional passive chopper as the demodulator in a low-noise low-power chopper amplifier for Coriolis acceleration sensing in CMOS-MEMS gyroscopes. At the transistor level, in addition to the implementation of the noise and power minimization techniques, a MOS-Bipolar device is successfully exploited for the robust dc biasing of the high-impedance sensing nodes.

Both single-axis and 3-axis integrated CMOS-MEMS accelerometer designs have been fabricated. The single-axis accelerometer prototype has a sensing capacitance of $4 \times 110 \, \text{fF}$ and a transducer sensitivity of 0.4 mV/g. Utilizing the DCA technology, the single-axis accelerometer achieves a noise floor of $50 \, \mu g/\sqrt{\text{Hz}}$ with 1 mW power dissipation. The DCA interface circuits have also been used for the integrated 3-axis accelerometer prototype, which achieves $12 \, \mu g/\sqrt{\text{Hz}}$ noise floor for X/Y-axis, and $110 \, \mu g/\sqrt{\text{Hz}}$ noise floor for Z-axis, with 1 mW power consumption for each axis.

The interface circuit for Coriolis acceleration sensing in CMOS-MEMS gyroscopes achieves a $20 \, nV/\sqrt{\text{Hz}}$ electronic noise at the Coriolis acceleration frequency band, and it dissipates a power of 1mW.
CHAPTER 1
INTRODUCTION

Monolithic micromachined inertial sensors including accelerometers and gyroscopes have grown rapidly into a major type of MEMS products over the past two decades. They have a wide range of applications in automotive, consumer electronics, computer system, navigation, sports and health care [1]. The trend towards miniaturization and higher performance results in electronics playing a more and more important role in integrated inertial sensors [2]. Furthermore, low-power consumption is becoming critical for inertial sensors to succeed in large volume consumer products. In this dissertation, first the fundamental limitations on low-power high-performance interface circuits design for capacitive inertial sensors are investigated. Then, design and optimization methodologies on low-noise and low-power interface circuits are presented. Finally, interface circuits simultaneously achieving both low noise and low power consumption are designed, and integrated CMOS-MEMS accelerometers and gyroscopes utilizing these circuits are demonstrated.

1.1 Overview of MEMS Inertial Sensors

1.1.1 MEMS Accelerometers

In the past two decades, various MEMS accelerometers have been reported and commercialized, employing a wide range of detection mechanisms, which include piezoelectric, piezoresistive, capacitive, resonance and tunneling [1]. Capacitive sensing is the dominant sensing mechanism in MEMS inertial sensors, since it has the advantages
of low temperature coefficients, low power consumption, low noise, low cost and potential compatibility with IC fabrication technology [3-10].

Microfabrication methods are generally classified into two main categories: bulk micromachining and surface micromachining, which both have been exploited to make MEMS inertial sensors. Bulk micromachining provides silicon-crystal silicon (SCS) microstructures and large proof masses for high resolution, high sensitivity and robustness, but typically requires complicated fabrication steps and wire-bonding to an ASIC chip [3, 4, 8, 9]. Surface micromachining, on the other hand, provides integrated electronics but suffers from light mass and large temperature dependence [5, 7, 11-13]. Because of their larger mass and larger sensing capacitance, bulk accelerometers have higher sensitivity and lower noise floor than thin-film accelerometers. For instance, a sub-μg/√Hz noise floor has been achieved using bulk micromachining [9], while the latest thin-film poly-silicon accelerometer still has a noise floor above 100 μg/√Hz [7].

With the goal to succeed in large volume applications, recent trends on MEMS accelerometers have been focused on achieving small size, low cost, low power dissipation and high resolution with dual-axis or 3-axis sensing capability. Table 1-1 summarizes previous work people have done in the area of MEMS accelerometers.

1.1.2 MEMS Gyroscopes

Micromachined gyroscopes are widely believed to be a third major MEMS product area beyond pressure sensors and accelerometers, but the design and fabrication of MEMS gyroscopes are far more complicated and challenging than MEMS accelerometers [1, 14]. In the past years, a variety of micromachined gyroscopes have been reported [15-
and the iMEMS Gyroscopes series from Analog Devices Inc. are currently the only commercially available integrated MEMS gyroscopes [17].

Table 1-1. Existing designs/products of MEMS accelerometers

<table>
<thead>
<tr>
<th></th>
<th># of axis</th>
<th>MEMS Technology</th>
<th>Interface Technology</th>
<th>Noise floor (μg / √Hz)</th>
<th>Power dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lemkin 1997 [7]</td>
<td>3</td>
<td>Poly surface, monolithic</td>
<td>Switched capacitor</td>
<td>110</td>
<td>45 mW (9 mA × 5 V)</td>
</tr>
<tr>
<td>Wu 2002 [5]</td>
<td>1</td>
<td>CMOS-MEMS, monolithic</td>
<td>Chopper stabilization</td>
<td>50</td>
<td>30 mW (6 mA × 5 V)</td>
</tr>
<tr>
<td>Kulah 2003 [8]</td>
<td>1</td>
<td>SCS bulk + ASIC</td>
<td>Switched capacitor</td>
<td>15</td>
<td>6.6 mW (1.32 mA × 5 V)</td>
</tr>
<tr>
<td>Amini 2004 [26]</td>
<td>1</td>
<td>SOI + ASIC, hybrid</td>
<td>Switched capacitor</td>
<td>110</td>
<td>6 mW (2.4 mA × 2.5 V)</td>
</tr>
<tr>
<td>ADXL103 [13]</td>
<td>2</td>
<td>Poly surface, monolithic</td>
<td>Chopper stabilization</td>
<td>110</td>
<td>3.5 mW (700 μA × 5 V)</td>
</tr>
<tr>
<td>MMA7260Q [27]</td>
<td>3</td>
<td>2 poly surface +ASIC, hybrid</td>
<td>Switched-capacitor</td>
<td>350</td>
<td>1.65 mW (500μA × 3.3 V)</td>
</tr>
<tr>
<td>KXP74 [28]</td>
<td>3</td>
<td>SCS + ASIC, hybrid</td>
<td>Switched capacitor</td>
<td>175</td>
<td>2.24 mW (0.8 mA × 2.8V)</td>
</tr>
<tr>
<td>LIS3L02 [29]</td>
<td>3</td>
<td>BiCMOS, hybrid</td>
<td>Switched capacitor</td>
<td>50</td>
<td>3.3 mW (1 mA × 3.3 V)</td>
</tr>
</tbody>
</table>

Various design methods and fabrication processes have been explored to improve the resolution and robustness of MEMS gyroscopes. However, little attention has been paid to achieve low-power consumption, which is becoming more and more important as MEMS gyroscopes recently start to be used in portable consumer products. Table 1-2 summarizes previous work that has been done in the area of MEMS gyroscopes.
Table 1-2. Existing designs/products of MEMS gyroscopes

<table>
<thead>
<tr>
<th></th>
<th>Technology</th>
<th>Interface Technology</th>
<th>Noise Floor ($^\circ$/sec/$\sqrt{Hz}$)</th>
<th>Power dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clark 1996 [16]</td>
<td>Ploy surface + ASIC Chopper stabilization</td>
<td>0.1</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>Jiang 2000 [21]</td>
<td>Ploy surface, monolithic Switched capacitor</td>
<td>3</td>
<td>50 mW (10 mA × 5 V)</td>
<td></td>
</tr>
<tr>
<td>Ayazi 2001 [15]</td>
<td>SCS bulk + ASIC Chopper stabilization</td>
<td>0.01</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>Geen 2002 [19]</td>
<td>Ploy surface, BiCMOS, monolithic Trans-capacitance amplifier</td>
<td>0.05</td>
<td>30 mW (6 mA × 5 V)</td>
<td></td>
</tr>
<tr>
<td>Xie 2003 [25]</td>
<td>DRIE CMOS-MEMS Chopper stabilization</td>
<td>0.02</td>
<td>N/A</td>
<td></td>
</tr>
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</table>

1.2 Integrated CMOS-MEMS Inertial Sensors

In recent years, large volume applications, especially those in portable consumer products, require accelerometers and gyroscopes with small size, low cost, low power consumption and high performance, which still are big challenges for the MEMS industry [30]. One potential solution to meet all the above requirements is the deep reactive-ion-etch (DRIE) CMOS-MEMS technology [10, 22, 25, 31]. Combining the advantages of both bulk micro-machining and surface micromachining, this technology simultaneously provides integrated electronics and large SCS proof mass. Integrated monolithic accelerometers and gyroscopes enabled by this technology have the potential to simultaneously achieve small size, low cost, low power dissipation and high robustness.

An integrated 3-axis CMOS-MEMS accelerometer has been reported in [10], and its mechanical structure design and the fabrication flow are shown in Figure 1-1 and Figure 1-2 respectively. In the structure design, the X- and Y-axis accelerometers share the same spring and proof mass, while the Z-axis sensing element is embedded in the
center of the proof mass with a torsional beam. With this unique structure design, only a single proof mass is needed for all the three axes. The maskless post-CMOS micromachining process shown in Figure 1-2 is used to release the 3-axis accelerometer. Most process steps in this post-CMOS micromachining are anisotropic and isotropic plasma etching of silicon or SiO₂, in which the top metal layer acts as the etching masks. Figure 1-2 shows the fabrication sequence of this process. The post-CMOS process starts with the backside etching to define the structure thickness, as illustrated in Figure 1-2(a). Then deep anisotropic SiO₂ etching is performed to open the isolation windows in step Figure 1-2(b). In Figure 1-2(c), a wet aluminum etching is used to remove the top metal layer (M4). After the removal of M4, anisotropic silicon DRIE and isotropic silicon etching are performed to undercut the isolation beams, as shown in step Figure 1-2(d). The removal of silicon underneath the isolation beams in this step isolates sensing fingers from silicon substrate. Next, in Figure 1-2(e), the second anisotropic SiO₂ etch opens the windows that define sensing fingers, springs and other mechanical structures. Finally, Si DRIE is performed again to etch through and release the accelerometer.

The major features of the inertial sensors made with the DRIE CMOS-MEMS technology are that they are CMOS-compatible and monolithic integrated sensors. Figure 1-3 shows the design and fabrication flow of CMOS-MEMS inertial sensors. Basically, there are four steps involved as follows:

1. Design of transducer structures and interface electronics (chip layout is sent to CMOS foundry);
2. IC fabrication in CMOS foundry;
3. After IC chips are returned, post-CMOS DRIE MEMS fabrication is applied at the clean room at the University of Florida;

4. Packaging, wire-bonding and testing.

Figure 1-1. Structure design of 3-axis CMOS-MEMS accelerometer.

Figure 1-2. Process flow of DRIE CMOS-MEMS technology.
Figure 1-3. Design flow of CMOS-MEMS inertial sensors.
1.3 Research Direction

The performance of MEMS inertial sensors is determined by three fundamental issues: transducer design and fabrication, sensing circuit design, and control system design. The fabrication of the MEMS transducer and control system design are out of scope of this research. This work is based on the existing DRIE CMOS MEMS process reported in [10, 22]. Due to the small sensing capacitance and low mechanical sensitivity from the sensing element, low-noise readout circuit design is very critical for the overall performance of integrated CMOS-MEMS inertial sensors.

There are three major capacitive sensing circuit architectures: continuous-time voltage (CTV) sensing using modulation/demodulation, continuous-time current (CTC) sensing based on trans-impedance amplifiers and trans-capacitance amplifiers, and switched-capacitor (SC) charge integration sensing. Both CTV and SC have been used in capacitive MEMS inertial sensors, with the former in [5, 10, 12, 13, 16, 18, 19, 22, 32], and the latter in [3, 4, 7-9, 20, 21, 26-29]. However, none of these designs has been reported to have both low electronic noise and low power consumption simultaneously, which are critical for MEMS inertial sensors to succeed in applications such as portable electronics and wireless sensors [30]. This research focuses on the design of interface circuits for CMOS-MEMS accelerometers and gyroscopes that achieve both low noise and low power consumption at the same time. The key problem that this project is targeting at can be stated as the following: Given the process limitations, how do we design an electronic subsystem that can achieve high performance with minimum power dissipation? Figure 1-4 shows a generic block diagram of the system under study.
1.4 Our Approach

To ensure high performance of the interface circuits while minimizing power dissipation, we first theoretically analyze fundamental limits on power consumption of capacitive sensing circuits with constraints on performance specifications including dynamic range (DR), gain, gain-bandwidth product (GBW) and linearity. Then, various interface circuits for capacitive sensing are investigated and compared, with the focus on their ability to achieve both low noise and low power at the same time. Based on this analysis and investigation, a new architecture, the dual-chopper amplifier (DCA), is proposed for capacitive sensing in CMOS-MEMS inertial sensors. The prototype circuit is designed and tested to verify our solution. Finally, monolithic CMOS-MEMS accelerometers integrated with the DCA interface circuits are designed and tested. In
addition, a low-noise and low-power interface circuit design for Coriolis acceleration sensing in vibratory CMOS-MEMS gyroscopes is studied in this work.

1.5 Dissertation Organization

This dissertation is divided into seven chapters. The motivation for this work, a background of MEMS inertial sensors, the DRIE CMOS-MEMS technology, and previous work on interface circuits for MEMS inertial sensors are introduced in the first chapter. Chapter 2 is an in-depth study and investigation of various capacitive sensing techniques used in MEMS accelerometers and gyroscopes, with the focus on their ability to achieve low noise level and low power consumption. In Chapter 3, design considerations to achieve both low noise and low power consumption are discussed. In Chapter 4, the dual-chopper amplifier (DCA) architecture is proposed, and its ability to achieve both low noise and low power are theoretically analyzed. In Chapter 5, detailed design and analysis of the DCA for CMOS-MEMS accelerometers are given, together with the experimental results of the interface circuits, and the integrated accelerometers. In Chapter 6, the methodology to design a low-power interface circuit for Coriolis acceleration sensing in CMOS-MEMS gyroscopes is described, where a chopper amplifier utilizing low-impedance-node chopping and dynamic element matching is designed, analyzed and tested. Chapter 7 concludes the dissertation with a summary, suggestions for future work on electronics design for MEMS inertial sensors, and an analysis of future directions.
CHAPTER 2
CIRCUIT TECHNIQUES FOR CAPACITIVE SENSING

Capacitive sensing is the dominant sensing scheme in MEMS inertial sensors, due to its advantages of low temperature coefficients, low power consumption, low noise, low cost and compatibility with IC fabrication technology. A variety of interface circuits, including both open-loop and close-loop configurations have been proposed in the past decades for capacitive MEMS accelerometers and gyroscopes. In open-loop configurations, the interface circuits only readout and/or amplify the sensed signal to a certain level [4, 5, 32]. While in close-loop configurations, the amplified sensing signal is fed back to control the mechanical sensing element and this is generally called closed-loop force-feedback control [7, 26]. For all these implementations, the front-end capacitive readout circuits are the critical part determining the overall performance of inertial sensors, which includes noise level, linearity, distortion, dynamic range and power dissipation.

In this chapter, the principle of capacitive position sensing is first introduced. Then, electronic noise in capacitive sensing circuits and techniques to reduce flicker noise are discussed. Finally, various capacitive sensing circuit techniques in MEMS inertial sensors are investigated, and their performance in noise power consumption are analyzed and compared.

2.1 Capacitive Sensing Principle

Figure 2-1 shows the principle of capacitive sensing based on capacitive voltage divider. \( x_0 \) is the gap of the comb fingers and \( C_0 \) is the sensing capacitance when the
movable inner plate is at the center. Assuming that the position change or displacement \( \Delta x \) is very small compared to \( x_0 \), the sensed voltage signal at the sensing node can be expressed as:

\[
V_{\text{sense}} = \frac{2C_0}{2C_0 + C_p} \frac{\Delta x}{x_0} V_m
\]  

(2.1)

where \( V_m \) is the amplitude of the modulation voltage, and \( C_p \) is the parasitic capacitance at the sensing node.

![Capacitive sensing principle](image)

Figure 2-1. Capacitive sensing principle.

Capacitive sensing is based on motion-induced charge transfer, which consequently generates an ac voltage or current. With different mechanical designs and wiring methods, the sensing capacitors from the transducer can be configured into a voltage source, a current source, or a charge source. Accordingly, there are three different topologies for the readout circuit: reading the voltage, reading the current, and reading the charge, as shown in Figure 2-2 (a), (b) and (c) respectively. Voltage sensing and current sensing can be easily implemented with continuous-time circuits, while it is more convenient to implement charge sensing in discrete-time switched-capacitor circuits. More details are discussed in section 2.3.
The mechanical sensing principle, damping and Brownian noise in accelerometers are reviewed in Appendix-A. In accelerometers, the acceleration bandwidth is limited by the resonant frequency $\omega_0$. And the transducer sensitivity is related to the natural resonant frequency $\omega_0$ as:

$$S_m = \frac{\ddot{x}}{\ddot{a}} = \frac{1}{\omega_0^2}$$  \hspace{1cm} (2.2)

where $\ddot{x}$ is displacement, $\ddot{a}$ is acceleration.

Combining equations (2.1) and (2.2), the transducer sensitivity of the accelerometer (at the inputs of readout circuits) is given by:

$$S_T = \frac{V_{\text{sense}}}{a} = \frac{2C_0}{2C_0 + C_p} \frac{V_m}{x_0} \frac{1}{\omega_0^2}$$  \hspace{1cm} (2.3)

As shown in Appendix-B, $S_T$ is about 1mV/g for the designed DRIE CMOS-MEMS accelerometers.
2.2 Noise in Capacitive Sensing Circuits

The overall performance of MEMS inertial sensors is determined by the transducer design, fabrication and the sensing circuits. Sensor output noise has two major noise sources: Brownian noise and electrical noise from the interface circuits. The Brownian noise is the thermal-mechanical noise, a random force generated by the Brownian motion of the ambient molecules. DRIE CMOS-MEMS inertial sensors have the advantages of providing low Brownian noise and high robustness. For the single-axis accelerometer with small dimension shown in Appendix-B, the Brownian noise $a_{n,m}$ is about $20 \mu g / \sqrt{Hz}$. As for the 3-axis accelerometer with larger dimensions, the Brownian noise is much smaller. For optimal design, the interface circuit must contribute an electronic noise comparable to $a_{n,m} \cdot S_r$. Detailed analysis on noise optimization is discussed in Chapter 3.

2.2.1 Electronic Noise Sources

Various electronic noise sources exist in the interface circuits. Figure 2-3 is a generic CTV capacitive circuit showing all noise sources and parasitic devices.

![Figure 2-3. Noise sources in capacitive sensing.](image-url)
Electronic noise comes from the following four sources: the thermal noise of the sensing node biasing resistance $i_{n,b}$, the thermal noise from the input transistor $i_{n,h}$, the flicker noise from the input transistor $i_{n,flicker}$ and noise from the load $i_{load}$. By designing the circuit properly, the noise contributed by the load and following stages can be minimized so that the total noise will be dominated by the input device. Therefore, $i_{load}$ is neglected in the following discussions.

Using long channel approximation, the power spectral densities (PSD) of the various noises are given by:

$$i_{n,h}^2(f) = 4YkTg_m = 4YkT\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (2.4)$$

$$i_{n,flicker}^2(f) = \frac{K_f I_D}{C_{ox} L^2 f} \quad (2.5)$$

and

$$i_{n,b}^2(f) = \frac{4kT}{R_b} \quad (2.6)$$

where $W$ and $L$ are the channel width and length of the MOSFET, $g_m$ is the transconductance of the MOSFET, $I_D$ is the bias current of the MOSFET, $k$ is the Boltzmann’s constant, $T$ is the temperature in Kelvin, $\mu_n$ is the carrier mobility, $C_{ox}$ is the gate capacitance per unit area, $K_f$ is the flicker noise coefficient, $R_b$ is the resistance value of the biasing resistance, and $f$ is the frequency at which the circuit is operated. The MOSFET thermal noise coefficient $\Upsilon$ is 2/3 for long channel transistors.
2.2.2 Circuit Techniques to Reduce Flicker Noise

For CMOS circuits in MEMS inertial sensors, flicker noise dominates in the frequency band of acceleration and rotation signals, which is typically less than a few kHz. So the low frequency flicker noise must be effectively removed for low-noise interface circuits design.

Autozeroing, correlated double sampling (CDS) and chopper stabilization (CHS) techniques are widely used in precision circuits to reduce offset and flicker noise [33]. In interface circuits for MEMS inertial sensors, CHS is used in continuous-time sensing, while CDS is used in switched-capacitor charge sensing circuits.

The principle of autozero (and CDS in SC circuits) is shown in Figure 2-4. The offset and flicker noise cancellation is done in two phases. In sampling phase $\Phi_1$, the offset and $1/f$ noise are measured and sampled on $C_{os}$; and in amplification phase $\Phi_2$, the sampled offset and $1/f$ noise are subtracted from the input signal. The transfer function of the noise to the output is just a high pass filtering.

![Figure 2-4. Principle of autozero (CDS) technique.](image)
Figure 2-5 shows the principle of chopper technique. The input signal $V_{in}$ is modulated to the chopping frequency, amplified and demodulated back to the baseband. The offset and flicker noise are modulated only once and appear at the chopping frequency and its odd harmonics, and these frequency components are removed by a low-pass filter. In the time domain, the input signal $V_{in}$ is periodically inverted by the first chopper; after amplification, the inverted and amplified signal is inverted for the second time, resulting back in the baseband signal. The offset and flicker noise are periodically inverted only once and therefore appears as a square wave at the output, which can be finally low-pass filtered out.

Figure 2-5. Chopping principle including signals in frequency and time domain.
2.3 Review of Capacitive Sensing Circuits for MEMS Inertial Sensors

There are three types of readout circuits for capacitive sensing: switched-capacitor (SC) charge integration amplifier, continuous-time (CTC) current readout with transimpedance amplifier (TIA), and continuous-time voltage readout (CTV). The CTV readout can be realized by three approaches: unit-gain buffer, capacitive feedback architecture, and open-loop architecture. The SC amplifiers can have offset cancelled with either input-offset storage (IIS) or output-offset storage (OOS).

2.3.1 Dc Biasing in Continuous-Time Sensing Circuits

In continuous-time sensing, a voltage divider is formed by the sensing capacitors with the ac modulation voltages applied to the modulating electrodes. Square-wave clocks are commonly used as the modulation voltages for their easy generation. A biasing circuit is needed to provide stable dc bias at the sensing nodes. The noise contribution from the biasing resistance $R_b$ is shown in Figure 2-6. A half capacitive bridge is configured into a voltage divider in Figure 2-6(a), with its equivalent small signal model shown in Figure 2-6(b). Figure 2-6 (c) shows the noise contributed by $R_b$. At the modulation frequency $f_M$, the noise voltage $v_n$ due to $R_b$ is given as:

$$v_n^2(f_M) = \frac{4kTR_b}{(1 + 2\pi f_M R_b (2C_0 + C_p))^2}$$

(2.7)

In order to avoid signal attenuation and minimize the thermal noise from $R_b$, the resistance value of $R_b$ must be chosen such that:

$$R_b \geq \frac{1}{2\pi f_M (2C_0 + C_p)}$$

(2.8)

Where $f_M$ is the chopping frequency, $C_0$ is the sensing capacitance, and $C_p$ is the parasitic capacitance at sensing node.
Figure 2-6. Dc biasing of continuous time sensing. (a) Capacitive sensing with voltage divider. (b) Equivalent small-signal circuit. (c) Noise contributed by $R_b$.

Since $C_0$ is very small, $R_b$ normally needs to have incremental impedance in $\text{M}\Omega$-$\text{G}\Omega$ range. In practice, pure resistors are rarely used because large resistors occupy large silicon area and introduce large parasitic capacitance, which reduces the signal-to-noise ratio (SNR). A number of devices with high ac impedance have been used as the bias devices, including reverse-biased diodes, sub-threshold MOS FETs, long-channel MOS FETs, switch-biasing, and MOS-Bipolar device pseudo-resistors [5, 12, 19, 32, 34, 35]. The advantages and disadvantages of these biasing options are summarized in Table 2-1.

In the following sections, the biasing device is only drawn as a large resistor in all the figures.

<table>
<thead>
<tr>
<th>Biasing technique</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse-biased diodes</td>
<td>Simple implementation</td>
<td>Signal distortion</td>
</tr>
<tr>
<td>Sub-threshold MOS FETs</td>
<td>Simple implementation</td>
<td>Difficult to control</td>
</tr>
<tr>
<td>Long-channel MOS FETs</td>
<td>Good linearity</td>
<td>Complexity, small cross voltage</td>
</tr>
<tr>
<td>Switch-biasing</td>
<td>Stable biasing, simple</td>
<td>Large charge injection, signal distortion</td>
</tr>
<tr>
<td>MOS-bipolar device</td>
<td>Large cross voltage</td>
<td>Long settling time</td>
</tr>
</tbody>
</table>
In SC charge sensing circuits, the sensing nodes are periodically reset to a dc level through a switch. Therefore, no dc bias problem exists in these circuits.

2.3.2 Continuous-Time Voltage Sensing

There are three topologies using continuous-time voltage (CTV) sensing: (a) unit-gain voltage buffer, (b) chopping amplifier with capacitive feedback, and (c) open-loop differential chopper amplifier.

2.3.2.1 Unit-gain voltage buffer

Unit-gain buffers are used as readout circuits in [15, 34]. The block diagram of a unit-gain voltage buffer readout circuit is shown in Figure 2-7(a). In this architecture, the output signal is given by

\[ V_{out} = \frac{2\Delta C}{2C_0 + C_p} V_m \]  

(2.9)

The circuit dc offset and the flicker noise are removed by the CHS technique. If the modulation frequency is larger than the flicker noise corner, only thermal noise of the circuit will contribute to the output noise. However, the sensed signal at the inputs of the readout circuit \( V_s \) is attenuated by \( C_p \) as:

\[ V_s = \frac{2\Delta C}{2C_0 + C_p} V_m \]  

(2.10)

SNR of this configuration is attenuated by \( C_p \). For technologies where \( C_p \) is much larger than \( C_0 \), the parasitic \( C_p \) can be bootstrapped as shown in Fig. 2-7(b). One potential problem with the bootstrapped buffer is that it will be unstable if the open-loop gain is equal or greater than 1. The voltage buffer will contribute extra noise and consume extra
power, so it is not a good architecture to achieve low noise level and low power consumption.

2.3.2.2 Chopper amplifier with capacitive feedback

Capacitive readout circuits utilizing chopper amplifiers with capacitive feedback have been used in MEMS accelerometers [36] and gyroscopes [16]. Figure 2-8 shows the block diagram of this topology, in which the output voltage is given by:

\[ V_{out} = \frac{\Delta C}{C_1} V_m \]  

(2.11)

Figure 2-7. Unit-gain buffer readout. (a) Voltage buffer. (b) Voltage buffer with bootstrapping.
Since an ac virtual ground is provided at the sensing node in this configuration, the sensed signal is parasitic capacitance-insensitive. It also offers accurate gain and good linearity. However, the SNR is still deteriorated by $C_p$, because the noise transfer function from the input to output is affected by $C_p$. In pure CMOS MEMS inertial sensors that have small sensing capacitance $C_0$, a chopping clock with a relatively high frequency is needed to effectively reduce the flicker noise. The high gain-bandwidth requirement of the amplifier in this feedback configuration results in a limit on the minimum achievable power consumption.

### 2.3.2.3 Open-loop differential chopper amplifier

Figure 2-9 shows the block diagram of an open-loop differential chopper amplifier. In this configuration, the sensed signal is sensitive to the parasitic capacitance $C_p$ at the sensing nodes, as in the voltage buffer without bootstrapping. For this reason, the open-loop architecture is undesirable if a large varying $C_p$ exists at the sensing node. It has been successfully used in CMOS-MEMS accelerometers [5, 12, 32, 35] and gyroscopes.
Since the wiring from sensing elements to the inputs of readout circuits is provided by metal layers in CMOS-MEMS process, $C_p$ is stable and with a value comparable to or smaller than the sensing capacitance $C_0$. So, the SNR attenuation introduced by $C_p$ is relatively small in these technologies. The topology has the potential to achieve both low power consumption and low noise, since high gain-bandwidth product requirement is not needed in open-loop amplifier, and high chopper frequency is achievable to effectively remove 1/f noise without consuming too much power. Some disadvantages exist in this configuration, such as gain inaccuracy, distortion with large input signals, and sensitivity to process variations and temperature drift.

![Figure 2-9. Open-loop differential chopper amplifier.](image)

### 2.3.3 Continuous-Time Current Sensing

In a continuous-time current sensing configuration, the displacement current from the sensing nodes is readout and converted into a voltage output by the readout circuits. There are two configurations: (a) trans-capacitance amplifier (TCA) and (b) trans-impedance amplifier (TIA), as shown in Figure 2-10 and Figure 2-11, respectively.
2.3.3.1 Trans-capacitance amplifier

In the TCA shown in Figure 2-10, the dc biasing of sensing nodes is set by a big resistance $R_b$ as described in section 2.3.1, and the signal is not sensitive to $C_p$. The output is given by:

$$V_{out} = \frac{\Delta C}{C_1} V_{ref}$$  \hspace{1cm} (2.12)

Low power consumption is achievable since the circuit amplifies signal at the baseband and the gain-bandwidth product of the amplifier is not high. However, flicker noise will be a serious problem in pure CMOS processes, since the readout circuit works only in the basband. Another disadvantage is that only ac capacitance changes can be sensed in this configuration. This topology has been used in ADI’s gyroscope products, where Biploar transistors are used in the Coriolis acceleration sensing circuits [19]. This is because ADI has BiCMOS process for its inertial sensor products.

![Figure 2-10. Trans-capacitance amplifier.](image)

2.3.3.2 Trans-impedance amplifier

Fedder showed a transimpedance amplifier for capacitive sensing in [34], with its topology shown in Figure 2-11. The circuit output is given by:
\[ V_{out}(f) = j2\pi f R_F \Delta CV_m \] (2.13)

For capacitive sensing, the transimpedance amplifier is a differentiator that has a high-pass frequency response. This architecture provides virtual ground and robust dc biasing at the sensing node in continuous-time. However, the noise performance of this topology is inferior to other topologies, since the white noise of the amplifier at high frequencies will be amplified by the amplifier, due to its high-pass transfer function.

![Trans-impedance amplifier](image)

Figure 2-11. Trans-impedance amplifier.

### 2.3.4 Discrete-Time Charge Sensing

In charge sensing, the capacitance change is converted to charge redistribution, which can be readout with discrete-time switched-capacitor (SC) circuits. Correlated double sampling (CDS) technique is widely used in SC circuits to cancel 1/f noise of the amplifier. Based on where to store the sampled offset and 1/f noise voltage in CDS, there are two different SC charge integration amplifier configurations: (a) SC amplifiers with input offset storage (IOS) [3, 4, 8, 26], and (b) SC amplifiers with output offset storage (OOS) [7, 20, 21], as shown in Figure 2-12 and Figure 2-13 respectively.
In Figure 2-12, during $\Phi_1$, the charges on sensing capacitors are reset to zero and the circuit offset (and low frequency 1/f noise) is stored on $C_{os}$. During $\Phi_2$, the circuit offset is subtracted and the sensed signal is amplified. In this configuration, the thermal noise from switching is determined by $\frac{kT}{C_0}$, and a relatively large $C_0$ is needed to reduce this noise component. Therefore, SC amplifiers with IOS are only used in MEMS accelerometers where large $C_0$ is achievable.

In Figure 2-13, the dc level of the charge integration amplifier is set during $t_1$, and the circuit offset (and 1/f noise) is stored into $C_{int}$ during $t_2$. During $t_3$, the offset is cancelled and the signal is amplified. In this configuration, the thermal noise from switching is determined by $kT/C_{int}$. Since $C_{int}$ can be made relatively large, so the $kT/C$ noise is effectively reduced, and also a small $C_0$ is allowed. A drawback of this topology is that a preamp is needed after the charge-integration amplifier, so it dissipates more power than the topology in Figure 2-12.

Figure 2-12. Switched-capacitor amplifier with IOS [4].
In both SC charge integration circuits, the output signal is given by:

\[ V_{out} = \frac{\Delta C}{C_{int}} V_m \]  

(2.14)

The SC readout circuits have good robustness, accurate gain and good linearity. However, the 1/f noise is reduced at the cost of folding back all the thermal noise of the amplifier back into the baseband. Therefore, its noise performance is worse than the continuous-time voltage sensing circuits.

2.4 Comparison of Different Capacitive Sensing Architectures

The noise performances of SC charge integration amplifiers, continuous-time voltage sensing, and continuous-time current sensing have been thoroughly studied in [6].

Due to their sample-and-hold nature, SC charge integration amplifiers suffer from two noise-related mechanisms. The first is kT/C noise from the sampling switches. Nevertheless, it can be effectively reduced when OOS is utilized for the CDS at the cost of more power dissipation, as illustrated in [7, 20, 21]. The other one is the thermal noise
folding effect, which is fundamental to SC circuits. During the sampling process, all noises in the pass-band will be folded back into the baseband.

In continuous-time circuits utilizing modulation and demodulation, if the modulation voltage is a pure sinusoid, there will be no noise folding effect. However, a square-wave clock is commonly used, so the noise folding effect exists due to the odd harmonics of the clock.

In the SC circuits, assume that $f_s$ is the sampling frequency and $BW$ is the bandwidth of the amplifier. Assume that the bandwidth $BW = Nf_s$, then the SNR reduction due to the noise folding is given as [6]:

$$\frac{SNR_{SC}}{SNR_0} = \frac{1}{N} \quad (2.15)$$

Figure 2-14 shows the noise folding effect in continuous-time voltage sensing circuits. Assuming $BW = (2N-1)f_m$, where $f_m$ is the modulation clock frequency, the SNR reduction due to noise folding is given as [6]:

$$\frac{SNR_{CTV}}{SNR_0} = \frac{\left[ \frac{8}{\pi^2} \sum_{n=1}^{N} \frac{1}{(2n-1)^2} \right]^2}{\frac{16}{\pi^2} \sum_{n=1}^{N} \frac{1}{(2n-1)^2}} \quad (2.16)$$

In the continuous-time trans-impedance amplifier (TIA), the white noise is amplified at high frequency, as shown in Figure 2-15. Therefore, the noise folding effect introduces more noise in the base band after demodulation than the continuous-time voltage sensing circuits.
Assuming $BW = (2N-1)f_m$, where $f_m$ is the modulation clock frequency. The SNR reduction in TIA is given as [6]:

$$\frac{SNR_{TIA}}{SNR_0} = \frac{\left[ \frac{8}{\pi^2} \sum_{n=1}^{N} \frac{1}{(2n-1)^2} \right]^2}{\frac{16}{\pi^2} N}$$

(2.17)
The comparison of SNR reduction due to the noise folding effect is shown in Figure 2-16, where the bandwidth is normalized with the modulation or sampling frequency ($BW/f_m$ or $BW/f_s$). It is clear that CTV sensing circuits offer at least 3 dB better SNR than their counterparts from other two architectures. Due to its inferior noise performance, TIA is not a good choice for capacitive MEMS inertial sensors.

Typically, $BW/f_m$ is about 10 to avoid much phase lag introduced by the amplifier in continuous-time sensing, while $BW/f_s$ is also about 5-10 in SC circuits to satisfy settling requirements. Since power dissipation is mainly determined by GBW requirements, when CTV and SC circuits have similar GBW requirements, they have similar power consumption when the clock frequency is the same.

Figure 2-16. Comparison of SNR reduction due to noise folding.
2.5 Summary

The principles of capacitive sensing and various sensing circuit technologies for capacitive MEMS inertial sensors are studied in this chapter. We have found that the open-loop CTV sensing has the potential to achieve both low noise and low power in integrated CMOS-MEMS accelerometers and gyroscopes.
CHAPTER 3
DESIGN CONSIDERATIONS FOR LOW NOISE AND LOW POWER

Low-noise and low-power design for the interface circuits is fundamentally constrained by the tradeoff between noise and power dissipation. In practice, it is very difficult to find an optimal design that can simultaneously minimize both noise level and power consumption. In this chapter, noise optimization methods are first introduced. Then, the fundamental tradeoff between noise and power dissipation is investigated, together with its impact on the design methodology for low-noise and low-power circuits. General techniques to minimize power consumption for conventional open-loop chopper amplifiers are also discussed. Finally, the design of a low-noise and low-power chopper amplifier for CMOS-MEMS accelerometers is presented.

3.1 Noise Optimization

The noise floor of inertial sensors is determined by three factors: the Brownian noise, transducer sensitivity and the electronic noise from interface circuits. For instance, the input-referred noise floor of accelerometers is given by:

\[
a_n = \sqrt{a_{nm}^2 + \frac{v_n^2}{S_T^2}}
\]

where \(a_{nm}\) is the Brownian noise from the sensing element, \(S_T\) is the transducer sensitivity, and \(v_n\) is the input-referred noise of the interface circuit.

The major parameters of the single-axis DRIE CMOS-MEMS accelerometer are listed in Table 3-1 (please see Appendix-B for its mechanical design specifications). The
sensing element has a transducer sensitivity \( S_r \) of about 1 mV/g, and a thermal-mechanical Brownian noise \( a_{n,m} \) of about 20 \( \mu g / \sqrt{Hz} \).

Table 3-1. Parameters of the single-axis accelerometer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>600( \mu )m \times 300( \mu )m</td>
</tr>
<tr>
<td>Proof-mass</td>
<td>12.58 ( \mu )gram</td>
</tr>
<tr>
<td>Spring constant (K)</td>
<td>18.12 N/m</td>
</tr>
<tr>
<td>Resonant frequency ( \omega_0 )</td>
<td>6 kHz</td>
</tr>
<tr>
<td>Quality factor (Q)</td>
<td>1.3</td>
</tr>
<tr>
<td>Comb-finger gap ( x_0 )</td>
<td>4 ( \mu )m</td>
</tr>
<tr>
<td>Sensing capacitance ( 4 \times C_q )</td>
<td>4 \times 110 fF</td>
</tr>
<tr>
<td>Interconnect capacitance ( C_p )</td>
<td>60 fF</td>
</tr>
<tr>
<td>Sensitivity ( S_r )</td>
<td>1 mV/g</td>
</tr>
<tr>
<td>Brownian noise ( a_{n,m} )</td>
<td>20 ( \mu g / \sqrt{Hz} )</td>
</tr>
</tbody>
</table>

3.1.1 System-Level Noise Optimization

At the system level, the optimal design requires that the equivalent noise level due to electronic noise from interface circuits must be about the same as the Brownian noise contributed by the sensing element. Otherwise, either the sensing element or the interface circuit will be over designed. For the interface circuit, over-design in noise level means wasting a lot of power. This optimization leads to:

\[
a_{n,m} = \frac{v_n}{S_r} \tag{3.2}
\]

and the overall noise floor of an optimally designed accelerometer should be:

\[
a_{n,\text{opt}} = \sqrt{2}a_{n,m} \tag{3.3}
\]

The optimization requires that the interface circuit for the single-axis accelerometer must achieve an input-referred noise of about 20 \( nV / \sqrt{Hz} \). To achieve such a low noise
level is very challenging in monolithic MEMS inertial sensors, since the minimum electronic noise is also limited by the sensing capacitance $C_0$ as shown below.

### 3.1.2 Electronic Noise Minimization

With given sensing capacitance $C_0$ and parasitic capacitance $C_p$, theoretically there is an optimum size of the input MOS transistors that minimizes the input-referred electronic noise at each frequency. The minimum electronic noise is determined by both the transducer design and the circuit technology. The detailed noise minimization method has been studied by Wu in [6], where the generic capacitive sensing circuit shown in Figure 3-1 is utilized for the analysis. The main conclusions are summarized in this section.

The optimal width of transistor M is found by making:

$$\frac{\partial a_n^2(f)}{\partial W} = 0$$

(3.4)

where $a_n^2(f)$ is the sensor noise density due to electronic noise.
If the electronic noise is dominated by flicker noise, the optimum width of MOSFET is given by:

\[ W_{opt} = \frac{2C_s + C_p}{\frac{2}{3}C_{ox}L + 2C_{ox}L_{ov}} \]  

(3.5)

where \( L_{ov} \) is the overlap of the gate to the source/drain.

And \( W_{opt} \) leads to:

\[ C_{gs} + C_{gd} = 2C_s + C_p \]  

(3.6)

If both the flicker noise and the thermal noise are considered, the optimum width of the transistor is smaller than the value given by (3.4). Simplified expressions of the optimal width and the capacitance relationship are given by:

\[ W_{opt}' = \eta \cdot \frac{2C_0 + C_p}{\frac{2}{3}C_{ox}L + 2C_{ox}L_{ov}} \]  

(3.7)

\[ C_{gs} + C_{gd} = \eta \cdot (2C_0 + C_p) \]  

(3.8)

where \( 1/3 < \eta < 1 \), and \( \eta \) is a coefficient dependent on \( W_{opt}' \). Equations (3.5) and (3.7) show that when the gate capacitance of the input MOSFET is at a value equal to or smaller than the total capacitance of the sensor and the interconnection parasitic, the minimum input-referred electronic noise is achieved. This noise optimization method is referred as optimum capacitance matching. And it is widely used in interface circuits design for monolithic CMOS-MEMS accelerometers and gyroscopes.

The sensing capacitance \( C_0 \) in DRIE CMOS-MEMS accelerometers and gyroscopes is very small, typically with a value of 100 fF to less than 1 pF. The small \( C_0 \) makes it a big challenge to design low-noise interface circuits, as the low frequency flicker noise is
the dominant factor in CMOS circuits in the acceleration and rotation signal band. Figure 3-2 shows the simulated results of the minimum noise level that can be achieved with a given sensing capacitance $C_\theta$. Transistor models for the TSMC 0.35 μm technology is used in the simulation, and $C_P$ is chosen as 60 fF. It is clear that the flicker noise corner is about 1 MHz when $C_\theta$ is in sub-pF range. This high flicker noise corner requires a high clock frequency in the chopper amplifier or the CDS circuit to effectively remove the 1/f noise.

Figure 3-2. Simulation results of minimum noise versus frequency.
3.2 Design for Both Low Noise and Low Power

3.2.1 Tradeoff Between Noise and Power

The thermal noise in circuits is physically fundamental and related to the power consumption. Using the long channel approximation, the minimum noise of the optimally-sized input MOSFET is given as:

\[ v^2_{n,min} = \frac{4\gamma kT}{g_m} = \frac{4\gamma kT}{\sqrt{2\mu_n C_{ox} W_{opt} I_D}} \]  \hspace{1cm} (3.9)

where \( I_D \) is the bias current of the transistor.

Equation (3.8) shows the tradeoff between noise level and power dissipation. On the one hand, increasing bias current reduces the noise floor. However, it is the least effective way to reduce noise, since a 2x reduction of noise floor requires 16x larger current. On the other hand, it is very effective to reduce power consumption by allowing a little bit higher noise than the minimum value.

When the velocity saturation effect of short-channel devices is concerned, the transconductance of actual short-channel devices is lower than that predicted by long-channel approximation. In the deep velocity saturation region, the transconductance of a MOSFET becomes:

\[ g_{m sat} = \mu C_{ox} E_c \]  \hspace{1cm} (3.10)

where \( E_c \) is the critical electric field.

Equation (3.9) shows that the transconductance reaches a saturated value and can no longer be increased by dissipating more bias current. In this case, the noise performance does not benefit any more from higher power consumption.
The fundamental noise-power tradeoff reveals that theoretically there should be an optimal design that can simultaneously achieve both low noise and low power dissipation. However, such an optimal design is hard to achieve in practice. One practical methodology is to design a circuit that meets the noise requirement with minimum power dissipation. Nevertheless, to avoid missing the noise specification, accurate noise modeling is needed in the design stage, which is a challenge to the modeling and characterization of the technology used by the circuits.

### 3.2.2 Choice of Circuit Architectures

The power dissipation in analog circuits are highly related to circuit topology and performance specifications including noise, gain, linearity, signal swing, process and temperature variations [41]. In real circuit implementations, a good balance among the performance specifications must be obtained.

As shown in chapter 2, by reducing noise folding, continuous-time voltage readout is superior in noise performance over switched-capacitor charge integration and TIA-biased current sensing. Furthermore, by avoiding the large gain-bandwidth product requirement in the capacitive feedback amplifiers, the open-loop chopper amplifier architecture also achieves lower power dissipation. Therefore, the open-loop chopper amplifier architecture is utilized in this work to simultaneously achieve both low noise and low power.

Single-stage amplifiers have the highest current efficiency compared with other topologies, so they normally can achieve very good noise and power performance. However, when implemented in open-loop configurations to save power, it is very difficult to meet other requirements, such as good linearity and high gain, which are highly desirable in interface circuits for capacitive MEMS inertial sensors.
Since they have more design freedoms, multi-stage chopper amplifiers become the natural choice for low-noise and low-power capacitive sensing circuits. In the multi-stage configurations, the first stage can be implemented in open-loop to achieve not only low noise and low power, but also good linearity and some gain to inhibit noises from the following stages. Once the low noise requirements are satisfied, the following stages can be optimally designed to minimize the overall power consumption, and at the same time seek a good balance among other performance specifications.

### 3.3 Power Minimization in Chopper Amplifiers

Chopper amplifier is intrinsically a time-variant system, so periodic-steady-state (PSS) analysis is needed to fully investigate its behavior, as shown in Figure 3-3(a). However, it is very difficult and tedious to perform PSS analysis with hand calculation. A simplified analysis is to investigate the performance of the amplification stages embedded between the two choppers, which can be applied to estimate the noise and power dissipation of the overall chopper amplifier, as shown in Figure 3-3(b). Since the signal is amplified around the chopping frequency, as long as the amplifier’s pass-band is several times higher than the chopping frequency, the conversion loss due to chopping is negligible. The gain of the signal is about the same of the gain in the pass band of the amplifier.

The power dissipation of an open-loop chopper amplifier can be minimized when the amplifier is implemented in a multi-stage cascaded configuration, rather than a single stage implementation. And Figure 3-4 shows the simple case of power minimization in multi-stage chopper amplifiers.
Figure 3-3. Analysis of chopper amplifier. (a) PSS analysis. (b) Simplified analysis.

$$A_v(s) = \frac{V_{out}(s)}{V_{in}(s)}$$

Figure 3-4. Optimization of open-loop chopper amplifier. (a) One-stage. (b) Multi-stage.
In the one-stage configuration, the gain is provided by a single amplification stage with a gain of $G$, while in the multi-stage configuration, the gain $G$ is equally distributed into $N$ cascaded amplification stages, each with a gain of $\sqrt[2N]{G}$. Assuming that all the amplification stages have the same 3-dB bandwidth $BW_{3\text{-}dB}=Mf_H$ ($M>>1$) and a single dominant pole, then their transfer functions can be expressed as follows:

$$H_{1\text{-stage}}(s) = \frac{G}{1 + \frac{s}{2\pi Mf_H}}$$  \hspace{1cm} (3.11)

$$H_{i\text{th}}(s) = \frac{\sqrt[2N]{G}}{1 + \frac{s}{2\pi Mf_H}}, 1 \leq i \leq N$$  \hspace{1cm} (3.12)

The multi-stage configuration has an overall transfer function as:

$$H_{\text{Multi-stage}}(s) = \frac{G}{(1 + \frac{s}{2\pi Mf_H})^N}$$  \hspace{1cm} (3.13)

Because $M >> 1$ and $f_H >> f_B$, where $f_B$ is the base bandwidth, so these two configurations provide the same gain to the signal. However, the phase lag introduced by the multi-stage configuration is $N$ times higher than that of the single-stage configuration. For $M=10$, each stage will introduce a phase lag about $5.7^\circ$. In order to avoid large phase lag in (3.13), normally two to three cascaded stages are used in real implementation for the multi-stage amplifier.

Based on the relationship between power consumption and GBW of the amplifier, and further assuming that the $N$ stages in the cascaded configuration have same bias and load conditions, the power dissipations of both configurations can be derived as follows.

For the single-stage amplifier:
\[ GBW_{1\text{-stage}} = \frac{g_{m1}}{2\pi C_{L1}} = Gm_f H \] (3.14)

where \( g_{m1} \) is the transconductance of the input transistors, and it is related to the bias current \( I_{ss1} \) and the overdrive voltage \( (V_{gs} - V_T) \) as:

\[ g_{m1} = \frac{I_{ss1}}{V_{gs} - V_T} \] (3.15)

Combining (3.14) and (3.15), we can get the relationship between the bias current and the GBW as:

\[ I_{ss1} = 2\pi Gm_f H C_{L1} (V_{GS1} - V_T) \] (3.16)

Similarly, the bias current of the multi-stage amplifier is given as:

\[ I_{ss2} = 2\pi N \sqrt[3]{Gm_f H C_{L2}} (V_{GS2} - V_T) \] (3.17)

And the power dissipations of these two configurations are:

\[ P_{1\text{-stage}} = V_{DD} I_{ss1} = 2\pi Gm_f H C_{L1} (V_{GS1} - V_T) V_{DD} \] (3.18)

and

\[ P_{N\text{-stage}} = V_{DD} I_{ss2} = 2\pi N \sqrt[3]{Gm_f H C_{L2}} (V_{GS2} - V_T) V_{DD} \] (3.19)

then the power consumption ratio of these two configurations is:

\[ \frac{P_{N\text{-stage}}}{P_{1\text{-stage}}} = \frac{C_{L2} (V_{GS2} - V_T)}{C_{L1} (V_{GS1} - V_T)} \cdot G^{1/N - 1} \cdot N \] (3.20)

The first term of (3.20) is about 1, depending on circuit implementations. Figure 3-5 shows the simulated power ratio of the two configurations with different gains and number of stages. As the gain is larger than 10, the multi-stage configuration can save power. It also shows that using more than 2 stages does not have much advantage than the 2-stage configuration.
In monolithic MEMS inertial sensors, $G \geq 10$ is generally required, because the sensed signal is usually very small. Therefore, the 2-stage chopper amplifier is the best choice to achieve both low noise and low power consumption.

### 3.4 A Low-Noise and Low-Power Chopper Amplifier Design

Based on the above analysis, we designed a 2-stage open-loop chopper amplifier that simultaneously achieves both low noise and low power dissipation for CMOS-MEMS accelerometers [32]. The architecture diagram of the circuit is shown in Figure 3-6. The first stage is optimized to achieve minimum noise and at the same time provide a moderate gain, while the second stage is designed to provide more gain and maintain large signal swing and good linearity. Both stages are implemented in open-loop configurations with a gain of about 20 dB for the first stage and 26 dB for the second stage. The offset of first stage is canceled by ac coupling, and the offset of the second
stage is reduced with a local dc-feedback embedded within this stage. With a 1 MHz modulation clock, this design achieves an input-referred noise of $24 \, nV/\sqrt{Hz}$ and a power consumption of 1 mW.

However, there are some drawbacks with this open-loop 2-stage chopper amplifier architecture for capacitive sensing. First, since both stages work in open-loop configuration, gain accuracy and linearity is sacrificed, especially for the second stage, where the sensed signal has already been amplified by the first stage. Second, since the signal is amplified all at the high frequency band, the minimum achievable level of power dissipation is limited by the gain-bandwidth requirements.

![Figure 3-6. A low-noise and low-power CHS for CMOS-MEMS accelerometer.](image)
3.5 Summary

In this chapter, the design considerations to achieve both low noise and low power dissipation are investigated. It is shown that conventional chopper amplifiers can simultaneously achieve both low noise and low power for capacitive sensing. However, its low-power capability is limited, since the signal is amplified at the relatively high chopping frequency range in monolithic MEMS inertial sensors.
CHAPTER 4
DUAL-CHOPPER AMPLIFIER FOR CAPACITIVE SENSING

In this chapter, the new dual-chopper amplifier (DCA) architecture for capacitive sensing is proposed and its ability to achieve both low noise and low power consumption is theoretically analyzed. First, the concept and operational principle of DCA are introduced. Then the applications of the DCA in capacitive MEMS accelerometers and gyroscopes are discussed. Finally, the abilities to achieve both low-noise and low-power for DCA and the conventional 2-stage chopper amplifier are compared. Besides its low noise and low power capability, the DCA also offers better linearity, better gain accuracy, and smaller residual offset than the conventional open-loop chopper amplifier architecture.

4.1 Dual-Chopper Amplifier Architecture

The low-power capability of conventional chopper amplifiers for monolithic capacitive CMOS-MEMS inertial sensors is limited, because 1-2 MHz chopping frequency is needed to effectively remove the flicker noise, resulting in a high gain-bandwidth product requirement on the amplification stages. The power consumption can be greatly reduced if a major part of the gain is achieved at a lower frequency (which is still much higher than the signal bandwidth) without deteriorating the noise performance. This is the basic idea of the DCA architecture proposed in this section. With this new architecture, both low noise and low power consumption can be achieved simultaneously in the capacitive sensing circuits.
4.1.1 Operation Principle of DCA

The concept of DCA is shown in Figure 4-1. Instead of using one chopping clock as in conventional chopper amplifiers, the two-stage DCA architecture employs two fundamental chopping clocks $\Phi_L$ and $\Phi_H$ as in the nested chopper amplifier reported in [40]. In order to keep the phase lag introduced to the signal very small and easily low-pass filter the even-order harmonics at chopping frequencies due to demodulation, the frequencies of the two clocks are chosen such that $f_B << f_L << f_H$, where $f_B$ is the input signal bandwidth. A new modulation clock $\Phi_M$ is applied to the sensing capacitive bridge. As shown in Figure 4-1, $\Phi_M$ can be considered as $\Phi_L$ chopped by $\Phi_H$. In this configuration, the input signal is modulated twice by $\Phi_L$ and $\Phi_H$, and the double-modulated signal is first amplified by the open-loop, high-bandwidth amplifier $A_I$ that is optimized to minimize the noise. $A_I$ is designed to have only small gain to consume low power and obtain good linearity. After first demodulated by $\Phi_H$, the signal is further boosted in a lower frequency band (around $f_L$) by a low-bandwidth amplifier $A_2$, which can be implemented in close-loop configuration to provide a moderate gain, consume low power and maintain large linear range. With this dual-chopping 2-stage configuration, low noise, low power, and a large dynamic range are achieved simultaneously.

The operations of DCA in both frequency domain and time domain are also shown in Figure 4-2. After the two input modulation choppers, the signal is modulated to frequency $mf_H \pm nf_L$ ($m$ and $n$ are odd numbers) at the input of the DCA, and after the first demodulation chopper, the signal is down-converted to $nf_L$ ($n$ is odd number). After the final demodulation chopper and the low-pass filter, the amplified signal is finally retrieved.
Figure 4-1. The concept of DCA.

Figure 4-2. Operation principle of DCA. (a) Operation principle. (b) Operation in frequency domain. (c) Operation in time domain.
4.1.2 Application of DCA in Capacitive Accelerometers

In CTV capacitive sensing, only one pair of complementary modulating voltages can be applied to the sensing capacitive bridge. Careful studies show that the new modulating clock $\Phi_M$ can be generated logically by an exclusive OR (XOR) of $\Phi_L$ and $\Phi_H$. In this way, $\Phi_M$ can be considered as $\Phi_L$ chopped by $\Phi_H$, as shown in Figure 4-3(a). Then the two input choppers of the concept DCA can be merged into one when $\Phi_M$ is used as the modulation clock shown in Figure 4-3(b). In capacitive sensing applications, $\Phi_M$ can be directly applied to modulating electroplates of the sensing capacitors, and accordingly DCA can be utilized as the readout circuit, as shown in Figure 4-3(c).

![Figure 4-3](image)

Figure 4-3. Application of DCA in capacitive sensing. (a) Generation of mixed clock. (b) Combination of two input choppers. (c) DCA in capacitive sensing.
4.1.3 Application of DCA in Capacitive Gyrosopes

When a conventional chopper amplifier is explored to readout the Coriolis acceleration signal in vibratory MEMS gyroscopes, a dual-chopper-amplifier (DCA) configuration is formed automatically, as shown in Figure 4-4(a), where the dashed box shows the chopper amplifier for Coriolis acceleration sensing. Compared to the above DCA architecture (also shown in Figure 4-4(b)), the modulation clock $\Phi_M$ and the driving voltage $V_{drv}$, which has a frequency about 1 kHz to 20 kHz, are equivalent to the high chopping clock $\Phi_H$ and the low chopping clock $\Phi_L$ in the DCA, respectively. The only difference is that $V_{drv}$ is a sinusoidal voltage coming from the driving circuits in a gyroscope, while $\Phi_L$ is a square-wave clock in the capacitive accelerometers.

Figure 4-4. DCA in vibratory gyroscopes. (a) Block diagram of DCA in gyroscopes. (b) Block diagram of concept DCA.
4.2 Comparison between DCA and Conventional Chopper Amplifier

To illustrate how both low-noise and low-power are achieved simultaneously in DCA, a two-stage DCA and a conventional two-stage chopper amplifier (CHS) are compared. The architecture block diagrams of a two-stage chopper amplifier with high frequency chopping clock ($\Phi_H$) and the two-stage DCA utilizing one high ($\Phi_H$) and one low chopping clock ($\Phi_L$) are shown in Figure 4-5. The power minimization method shown in section 3.3 is applied to the 2-stage chopper amplifier shown in Figure 4-5(a).

4.2.1 Power Dissipation

To simplify the analysis, the frequency conversion properties in both the DCA and the chopper amplifier are neglected, this assumption is valid since $f_B<<f_L<<f_H$, so the conversion loss due to modulation and demodulation is very small, i.e., the mixer conversion gain is close to 1.

Assuming $f_B<<f_L<<f_H$ and both architectures achieve the same overall gain $G$ at the signal band, then $G_H*G_L=G$. One intuitive explanation of the lower power dissipation in DCA can be described first. In DCA, the first amplification stage $A_H$ provides gain at high frequency band (around $f_H$), while the gain from the second stage $A_L$ is achieved at a lower frequency band (around $f_L$). In the contrast, both amplification stages $A_{CHS1}$ and $A_{CHS2}$ in CHS only amplify the signal at the high frequency band (around $f_H$). So, when $A_{CHS1}$ and $A_H$ have similar GBW, but the GBW of $A_L$ can be much smaller than that of $A_{CHS2}$, therefore DCA can dissipates much less power. Their noise levels are about the same, since the noise from the first stage dominates the whole noise level in both topologies.
Figure 4-5. Comparison between conventional amplifier and DCA. (a) 2-stage chopper amplifier. (b) 2-stage DCA.

Assuming that both topologies in Fig. 4-5 are optimized for low power dissipation, and the amplification stages have the following transfer functions:

\[ H_{\text{CHS1}}(s) = H_{\text{CHS2}}(s) = \frac{\sqrt{G}}{s + \frac{1}{2\pi N_H f_H}} \quad (4.1) \]

\[ H_{\text{AH}}(s) = \frac{G_H}{s + \frac{1}{2\pi N_H f_H}} \quad (4.2) \]

\[ H_{\text{AL}}(s) = \frac{G_H}{s + \frac{1}{2\pi N_L f_L}} \quad (4.3) \]

So,
\[
H_{\text{CHS}}(s) = \frac{G}{s(1 + \frac{s}{2\pi N_H f_H})^2}
\]  \tag{4.4}

and

\[
H_{\text{DCA}}(s) = \frac{G}{(1 + \frac{s}{2\pi N_H f_H})(1 + \frac{s}{2\pi N_L f_L})}
\]  \tag{4.5}

Then power consumption of DCA \(P_{\text{DCA}}\) can be expressed as:

\[
P_{\text{DCA}} = 2\pi N_H f_H V_{DD} C_H (V_{GS-H} - V_T)(G_H + \frac{G N_L f_L C_L}{N_H f_H C_H V_{GS-H} - V_T})
\]  \tag{4.6}

Where,

- \(f_H\): high chopping frequency,
- \(f_L\): low chopping frequency,
- \(N_H f_H\): 3-dB bandwidth of \(A_1\),
- \(N_L f_L\): 3-dB bandwidth of \(A_2\),
- \(C_H\): load capacitance of \(A_1\),
- \(C_L\): load capacitance of \(A_2\),
- \(G_H\): gain of \(A_1\) at frequency around \(f_H\),
- \(G\): overall gain of the DCA at signal band,
- \(V_{GS-H}\): gate-source voltage of input transistors of \(A_H\),
- \(V_{GS-L}\): gate-source voltage of input transistors of \(A_L\),
- \(V_T\): threshold voltage of input transistors.

When the first stage of DCA has a gain \(G_H\) of

\[
G_H = \sqrt{\frac{N_L f_L C_L V_{GS-L} - V_T}{N_H f_H C_H V_{GS-H} - V_T} G}
\]  \tag{4.7}
the DCA achieves the minimum power dissipation $P_{DCA(min)}$ as given by:

$$P_{DCA(min)} = K \sqrt{\frac{N_L f_L}{N_H f_H} \frac{C_L}{C_H} \frac{V_{GS-L}}{V_{GS-H}} - V_T} G$$  \hspace{1cm} (4.8)$$

Similarly, the minimum power dissipation of the conventional two-stage chopper amplifier can be derived as:

$$P_{CHS(min)} = K' \sqrt{\frac{C_2}{C_1} \frac{V_{GS-2}}{V_{GS-1}} - V_T}$$  \hspace{1cm} (4.9)$$

Assuming that $A_{CHS1}$ and $A_H$ have the same 3-dB bandwidth, then $N=N_H$ and $K=K'$. And the ratio of the minimum achievable power dissipation of the two architectures can be expressed as:

$$\frac{P_{DCA(min)}}{P_{CHS(min)}} = \sqrt{\frac{N_L f_L}{N_H f_H} \frac{C_L}{C_H} \frac{V_{GS-L}}{V_{GS-H}} - V_T}$$  \hspace{1cm} (4.10)$$

If the CHS and DCA have similar loads, then (4.10) can be further simplified as:

$$\frac{P_{DCA(min)}}{P_{CHS(min)}} = \sqrt{\frac{N_L f_L}{N_H f_H}}$$  \hspace{1cm} (4.11)$$

And now it is clear that DCA can save power by providing some gain at a lower frequency band in the second stage. The power saving is directly related to the reduction of the 3-dB bandwidth in the low frequency band amplification stage.

### 4.2.2 Noise Level

As shown in Fig. 4-5(a) and 4-5(b), the two amplification stages in CHS introduce input-referred noise of $v_{n1}^2$ and $v_{n2}^2$ at the chopping frequency $f_H$, while the two stages in DCA introduce input-referred noise of $v_{nH}^2$ at $f_H$ and $v_{nL}^2$ at $f_L$ respectively. The final output noise spectrum density of these two architectures can be expressed as:
Comparing (4.12) and (4.13), we can see that these two architectures have about the same noise level since $v_{n1}$ is close to $v_{nH}$, and at the same time $G_H$ of the first stage in DCA is comparable to $\sqrt{G}$.

4.3 Noise and Power Optimization in DCA

The electronic noise minimization technique introduced in section 3.1 can be utilized to design the first stage of DCA. To simultaneously achieve both low noise and low power dissipation in DCA is equivalent to maximize the SNR to the power consumption ratio.

Since SNR is inversely proportional to the noise density and signal bandwidth, i.e.

$$SNR \propto \frac{1}{v_n^2BW}$$

(4.14)

where BW is 3-dB bandwidth and $v_n^2$ is the input-referred noise density.

So,

$$\frac{SNR}{P} \propto \frac{1}{v_n^2P}$$

(4.15)

Combining equations (4.6) and (4.13), we then get the noise density-power product as:

$$v_{no}^2P = 2\pi N_H f_H V_{DD} C_H G^2 (V_{GS-H} - V_T) (G_H + \frac{G}{G_H} N_H f_H V_{GS-H - V_T}) (1 + \frac{1}{G^2} v_{nH}^2)$$

(4.16)
where,

\[ v_{nH}^2, \text{ input-referred noise density of } A_H \text{ at } f_H. \]

\[ v_{nL}^2, \text{ input-referred noise density of } A_L \text{ at } f_L. \]

The goal of an optimal DCA design is to minimize \( v_n^2 P \). When all other design parameters are given except \( G_H \) in equation (4.16), there exists one optimal value of \( G_H \) with which the power-noise density-product can be minimized. The optimal value of \( G_H \) can be obtained by:

\[
\frac{\partial (v_n^2 P)}{\partial G_H} = 0 \tag{4.17}
\]

And this optimization technique is used in the DCA prototype design in Chapter 5.

### 4.4 Summary

A new Dual-Chopper Amplifier (DCA) architecture for capacitive sensing is proposed and its ability to achieve both low noise and low power consumption is theoretically analyzed. Besides its capability to achieve both low noise and low power consumption simultaneously, the DCA also offers better linearity, better gain accuracy, and smaller residual offset than the conventional open-loop chopper amplifier architecture.
In this chapter, the detailed design of the low-noise and low-power Dual-Chopper Amplifier (DCA) for capacitive sensing in CMOS-MEMS accelerometers is first introduced. Then experimental results of the DCA prototype will be presented. Finally, the test and characterization results of the integrated single-axis and 3-axis CMOS-MEMS accelerometers will be given. Compared with available solutions of interface circuits in MEMS accelerometers, the DCA achieves both low noise and low power consumption simultaneously. In addition, it also offers better linearity, smaller residual offset than the conventional open-loop chopper amplifier readout circuits.

5.1 Architecture

Figure 5-1 shows the block diagram of the fully-differential DCA for capacitive CMOS-MEMS accelerometers. A fully differential capacitive bridge is formed by the mechanical sensing capacitor pairs $C_s \pm \Delta C_s$. Typically the acceleration signal bandwidth $f_B$ is about a few kHz, so the two chopping clock frequencies are chosen as $f_H = 1$ MHz and $f_L = 20$ kHz to ensure that $f_B << f_L << f_H$. The modulating clock $\Phi_M$ is generated with a logic exclusive OR (XOR) of $\Phi_L$ and $\Phi_H$. The modulation amplitude is controlled by the reference voltages $V_{refp}$ and $V_{refn}$. The high-bandwidth amplifier $A_1$ is implemented with a small-gain, open-loop configuration to save power and keep distortion very low since the maximum input signal is only a few mVs. The low-bandwidth amplifier $A_2$ is implemented in a close-loop configuration with capacitive feedback to provide accurate
gain, good linearity and large signal swing. The dc offset of $A_I$ is cancelled by ac coupling. The residual offset of this DCA is determined by the low chopping frequency $\Phi_L$. The sensor offset can be cancelled by tuning $V_{os+}$ and $V_{os-}$.

One low-pass filter (LPF) is added after the first demodulator to reduce the cyclostationary noise, which is generated by the chopping operation of the stationary noise from $A_I$. As shown in Figure 5-2, the cut-off frequency of the LPF is chosen as 200 kHz so that the signal is not attenuated, and at the same time the cyclostationary noise is effectively removed.

Figure 5-1. Architecture diagram of low-noise and low-power DCA.
5.2 Optimization for Low-Noise and Low-Power

The optimization method introduced in section 4.3 is exploited here to optimize the gain of the first stage $A_1$, so that the overall SNR/power ratio of the DCA is maximized. This optimization is equivalent to minimize the power-noise density-product given as follows:

$$v_n^2(f)P = 2\pi N_H f_H V_{DD}(V_{GS-H} - V_I)C_H \left( G_H + \frac{G}{N_H f_H C_H} V_{GS-L} - V_T C_L \right) \left( 1 + \frac{1}{G_H^2 \nu_{nH}^2} \right) v_{nH}^2$$

where $v_{nH}^2$ is the input-referred noise density, and $P$ is the power dissipation of the DCA.

In the design specifications, a maximum signal of 10 mV is assumed at the inputs of the DCA, and the output of the second stage $A_2$ has a 4-Vpp swing with 3.3V supply voltage. Therefore, the overall gain ($G$) of the DCA is designed as 200. Design trade-offs regarding noise, linearity and accuracy lead to the following relationships between the design parameters of $A_1$ and $A_2$:

$$v_{nl} = 5 - 6v_{nH}$$

Figure 5-2. Cyclostationary noise reduction by LPF. (a) Signal and noise before the first demodulator. (b) Signal and cyclostationary noise after the first demodulator. (c) Frequency response of LPF. (d) Signal and noise after LPF.
\[
\frac{C_L}{C_H} = 2
\]  
(5.3)

\[
K = \frac{N_L f_L (V_{GS-L} - V_T)}{N_H f_H (V_{GS-H} - V_T)} = 0.2 \sim 0.4
\]  
(5.4)

where \( K \) is a coefficient determined by the 3-dB bandwidths and overdrive conditions of the two stages.

Applying equation (4-17), the minimum value of \( v_n^2(f)P \) is obtained when \( G_H \) has the optimal value as:

\[
G_{H,\text{opt}} = \sqrt[\sqrt{G}]{\frac{N_L f_L}{N_H f_H} \frac{C_L}{C_H} (V_{GS-L} - V_T)}
\]  
(5.5)

Substituting (5.3) and (5.4) into (5.5), the optimal gain of \( A_1 \) can be obtained.

Figure 5-3 shows the simulated relationship between \( G_H \) and the minimum achievable \( v_n^2(f)P \), where \( N_H f_H = 10 \text{ MHz} \), \( V_{GS-H} - V_T = 0.1 \text{ V} \), \( C_H = 1 \text{ pF} \), and \( v_{na} = 10 \text{ nV/}\sqrt{\text{Hz}} \) are used in the simulation. It is clear that when \( G_H \) has a value of about 10, the minimum noise-power product can be achieved in the DCA circuit.

![Figure 5-3. Relationship between \( G_H \) and noise-power-product.](image-url)
5.3 Transistor Level Design of the DCA

5.3.1 Clock Generation

The diagram of the clock generation of $\Phi_L$, $\Phi_H$ and $\Phi_M$ is shown in Figure 5-4, where the main clock is provided off-chip. $\Phi_H$ is a buffered copy of the main clock, and $\Phi_L$ is generated from the main clock by a frequency divider, with $T_L = 50 \times T_H$. The new modulation clock $\Phi_M$ is generated by $\Phi_L$ XOR $\Phi_H$. The frequencies are chosen as $f_H = 1$ MHz and $f_L = 20$ kHz. Digital buffers with proper sizes are used for $\Phi_L$, $\Phi_H$ and $\Phi_M$ to drive large capacitive loads.

All the clocks including $\Phi_M$, $\Phi_L$, $\Phi_H$ and their complements are non-overlap clocks, and the sub-circuit shown in Figure 5-5 is used to generate the non-overlap clocks.

Figure 5-4. On-chip clock generation of $\Phi_L$, $\Phi_H$ and $\Phi_M$
Figure 5-5. Sub-circuit to generate non-overlap clock.

5.3.2 Dc Biasing Circuit

The large dc biasing resistors $R_{b1}$, $R_{b2}$ and the feedback resistor $R_F$ are provided with the MOS-bipolar device pseudo-resistors [42], as shown in Figure 5-6. The MOS-bipolar device pseudo-resistor achieves an incremental resistance of more than 1 GΩ when the cross voltage is less than 0.3 V. $R_F$ is formed by three MOS-bipolar devices connected in series to allow large signal swing of about 2 V. The parasitic capacitance introduced by the MOS-bipolar pseudo-resistor is in the order of several fF, and it is negligible compared with the sensing capacitance and the interconnect capacitance.

The dc settling behavior of the sensing node ($V_X$) biased with the MOS-Bipolar device ($R_b$) is shown in Figure 5-7. In Figure 5-7(a), $C_{tot}$ is the total capacitance at the sensing node. Figure 5-7(b) shows that $V_x$ settles to the biasing voltage $V_B$ in a long time because the large resistance from $R_b$ results in a large time constant. However, due to the non-linear behavior of $R_b$, $V_x$ settles into $V_B-0.5V$ very fast, typically within about 0.1 ms to 0.2 ms, as shown in Figure 5-7(c). For a stable operation of the DCA circuit, a wide common-mode input range (about 1V) for the first stage is required.
Figure 5-6. DC bias resistors implemented with MOS-Bipolar device.

Figure 5-7. Settling of dc bias. (a) Dc biasing of sensing node. (b) Fully settled. (c) Settling to \( V_b - 0.5V \).
5.3.3 Chopper Demodulators

For chopper amplifiers, the residual offset is mainly due to the nonidealities of the input modulators. In the DCA architecture, two demodulation choppers are involved. After the first demodulator (the high frequency demodulator), the remaining part of the DCA functions just like a conventional chopper amplifier with the low frequency chopping clock. Therefore, careful design is needed to reduce the residual offset introduced by the charge injection mismatch from the high frequency chopper demodulator. In this design, the high-frequency chopper demodulator and the low-frequency chopper demodulator are implemented differently, as shown in Figure 5-8. The switches in the high-frequency demodulator are implemented as a single NMOS transistor with two half-sized dummy switches on both sides to reduce the charge injection effect, as shown in Figure 5-8 (a). The switches in the low-frequency demodulator are implemented as CMOS transmission gates to allow large signal swing, as shown in Figure 5-8(b).

Figure 5-8. Implementation of chopper demodulators. (a) High-frequency demodulator. (b) Low-frequency demodulator.
5.3.4 Amplifier $A_1$

Figure 5-9 shows the schematic of the high-bandwidth amplifier $A_1$. PMOS FETs are used for the input pair $M_1$ and $M_2$ due to their lower flicker noise corner. The minimum length is used for $M_1$ and $M_2$, while the width is optimally sized with respect to the sensing capacitance $C_s$ and the parasitic $C_p$ (section 3.1.2). Cascoded transistors $M_3$ and $M_4$ are used to reduce the miller effect. Diode-connected transistors $M_5$ and $M_6$ are used as the active load, with their dc biasing current partially bypassed by current sources $M_7$ and $M_8$, so the effective small signal gain can be boosted without requiring very low W/L ratio of the load transistors $M_5$ and $M_6$. With a 0.5 pF load, the first amplifier achieves a gain of 20 dB with a 10 MHz 3-dB bandwidth with a sink current of 120µA. Its input-referred noise is $12 \, nV / \sqrt{Hz}$ at 1 MHz.

![Figure 5-9. Schematic of amplifier $A_1$.](image-url)
5.3.5 OTA in Amplifier A2

The OTA used in the capacitive feedback of the second amplifier A2 is implemented with a fully differential folded-cascode operational trans-conductance amplifier (OTA), with its schematic shown in Figure 5-10. Long-channel large-width transistors are used for the input pair M1 and M2 to achieve a flicker noise corner of about 10~20 kHz. With a 130µA biasing current, it achieves open-loop gain of 80 dB with a 20 MHz unit-gain frequency. The phase margin is about 70º. In the close-loop configuration, A2 achieves an accurate gain of 26 dB with $C_F = 250 \, \text{fF}$ and $C_I = 5 \, \text{pf}$.

Figure 5-10. Schematic of folded-cascode OTA used in A2.
5.3.6 Low-Pass Filter after the First Demodulator

The schematic of the low-pass filter following the first demodulator is shown in Figure 5-11. Source degeneration is utilized in the input pair to achieve good linearity. It is a first-order low-pass filter with a cut-off frequency of 200 kHz and a linear input range of 300 mV. The gain of the LPF is about 1. The low pass capacitor $C_{lp}$ has a value of 6 pF. No off-chip large capacitor or resistor is needed in this design.

![Schematic of the low-pass filter after the first demodulator.](image)

Figure 5-11. Schematic of the low-pass filter after the first demodulator.

5.3.7 Biasing Circuit

The dc conditions of all building blocks in the DCA are established with the biasing circuit shown in Figure 5-12. The transistors in the DCA are all biased at the saturation region. Low-voltage cascoded current mirrors [43] are used to bias the gates of
the NMOS and PMOS current source transistors of the DCA. The gates of the NMOS cascode transistors are biased with a string of devices that are operated in their linear regions [44]. Similarly, the gates of the PMOS cascode transistors are biased by a string of devices in their linear regions. Small transistors MN and MP are used to ensure that the bias circuit settles to the desired operating point. Non-minimum channel lengths are used for the transistors in order to reduce the influence of channel length modulation on the bias voltages. The operating conditions in the bias circuit are established with an external reference current, $I_b$, which is 20\( \mu \)A in this design.

![Schematic of the biasing circuit.](image)
5.4 Simulation of the Dual-Chopper Amplifier

The transistor level design of each building block and the whole DCA is verified with circuit simulator Spectre provided by Cadence. Transistor models (BSIM3v3) for TSMC 0.35 μm process are used. The sensing capacitance \( C_s \) of 150 fF and parasitic \( C_p \) of 60 fF are assumed in the simulation.

Simulation results show that \( A_1 \) achieves a gain of about 20 dB at 1 MHz, while the input-equivalent noise level is \( 12 \, \frac{nV}{\sqrt{Hz}} \). The 3-dB bandwidth of \( A_1 \) is about 10 MHz with a load of 0.5 pF, and its flicker noise corner is at about 1 MHz. The low-frequency close-loop amplification stage \( A_2 \) provides a gain of 26 dB and input-referred noise of about \( 70 \, \frac{nV}{\sqrt{Hz}} \) at the low chopping frequency \( f_L \).

Conventional SPICE-like simulators cannot provide ac and noise analysis for circuits with periodic operating points, such as CHS and SC circuits. Therefore, the periodic-steady-state (PSS) analysis provided by the SpectreRF simulator is utilized to simulate the DCA circuit. However, the PAC, PXF and PNoise analysis in SpectreRF can only simulate frequency-conversion circuits with one main clock. So, special handling is used in the simulation of the DCA, as shown in Figure 5-13. The DCA in Figure 5-13(a) is decomposed into two separate conventional chopper amplifiers, one amplifier with high chopping clock \( \Phi_H \) and the other amplifier with low chopping clock \( \Phi_L \), as shown in Figure 5-13(b). These two sub-circuits are simulated independently with SpectreRF to obtain their gain and noise. Finally the gain and noise of the overall DCA can be obtained through the equivalent circuit, as shown in Figure 5-13(c).
Assuming that $A_1^*$, $A_2^*$, $v_{n1}^*$ and $v_{n2}^*$ are the equivalent gains and noises of the two independent chopper amplifiers shown in Figure 5-13(b), the gain $A_{DCA}$ and noise $v_{n-DCA}$ of the DCA can be expressed as:

$$A_{DCA} = A_1^* A_2^*$$  (5.6)

$$v_{n-DCA} = \sqrt{v_{n1}^2 + \left(\frac{v_{n2}}{A_1^*}\right)^2}$$  (5.7)

Figure 5-13. Simulation of DCA with SpectreRF. (a) Block diagram of DCA. (b) Simulation of two chopper amplifiers. (c) Equivalent DCA with $A_1^*$ replacing $A_1$ and the high frequency demodulator.
The PSS simulation results of $A_1^*$ and $v_{n_1}$ of chopper amplifier $A_1$ are shown in Figure 5-14, where the signal is at frequency around 20 kHz. Figure 5-15 shows $A_2^*$ and $v_{n_2}$ from $A_2$, where the signal is at baseband from dc to $f_B$. The overall gain $A_{DC4}$ and noise $v_{n-DC4}$ of the DCA readout circuit are shown in Figure 5-16. The gain of the DCA is 46 dB and the input-referred noise is about $15 \text{nV/√Hz}$ in the acceleration bandwidth.

![Figure 5-14. PSS simulation results of $A_1$ with chopping clock $Φ_H$.](image)

![Figure 5-15. PSS simulation results of $A_2$ with chopping clock $Φ_L$.](image)
In the simulation, a power supply of 3.3 V is used, and the DCA draws a current of 300 \( \mu \)A. So the power consumption of the DCA is only 1.0 mW.

### 5.5 Implementation of the DCA Prototype

The prototype of the DCA capacitive sensing circuit has been implemented in the TSMC 0.35\( \mu \)m 4-M-2-P CMOS process and fabricated through MOSIS. With its layout shown in Figure 5-17, the DCA takes an area of 900 \( \mu \)m \( \times \) 400 \( \mu \)m. Figure 5-18 shows the layout of the accelerometer chip, where a 3-axis CMOS-MEMS accelerometer, a single-axis accelerometer, and one DCA interface circuit for each axis are integrated on a single chip. The accelerometer chip has a size of 3 mm \( \times \) 3 mm.

The accelerometer chip is released with the DRIE CMOS-MEMS technology reported in [10]. The photograph of a tested accelerometer chip is shown in Figure 5-19, where the released structure of the single-axis and the 3-axis accelerometer can be seen clearly.

Figure 5-16. PSS simulation results of DCA.
Figure 5-17. Layout of the prototype DCA circuit.

Figure 5-18. Layout of the accelerometer chip.
Chips for testing the single-axis accelerometer are wire-bonded in a 40-pin DIP package, while chips for the 3-axis accelerometer are wire-bonded in a 52-pin PLCC package. Some PCB boards have been made for testing both these accelerometers. On the main test board, a low-noise instrumentation amplifier (Model: AD623) converts the differential output signals from the testing chip to a single-ended signal. For the 3-axis accelerometer test and characterization, two separate PCB boards were made, one mounting board and one supporting board, as shown in Figure 5-20. In this configuration, the mounting board in which the 3-axis accelerometer is embedded can be made as small and light as possible, so its mechanical effect on the characterization results is minimized.
5.6 Experimental Setup

Equipments and instruments used in the test include a shaker table, a spectrum analyzer, an oscilloscope, a reference accelerometer, a function generator, power supplies and other supporting instruments. The major equipments used in the experiments are summarized in Table 5-1.

<table>
<thead>
<tr>
<th>Equipment name</th>
<th>Model</th>
<th>Key Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shaker + Amplifier</td>
<td>LDS V-408/PA-100E Amplifier</td>
<td>Frequency range: 5 Hz – 9 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Maximum acceleration: 10 g</td>
</tr>
<tr>
<td>Handheld Shaker</td>
<td>PCB Handheld shaker</td>
<td>Acceleration: 1 g</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency: 159.1 Hz</td>
</tr>
<tr>
<td>Reference Accelerometer</td>
<td>KISTLER-8638b5</td>
<td>Acceleration Range: ±5g</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency Range: 0-9 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sensitivity: 979 mV/g</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Accuracy: 1.0%</td>
</tr>
<tr>
<td>Spectrum Analyzer</td>
<td>SR-785</td>
<td>DC to 102.4 kHz bandwidth</td>
</tr>
<tr>
<td></td>
<td></td>
<td>90 dB dynamic range</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>TDS-2014</td>
<td>Sample Rates: 1 GS/s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bandwidth: 100 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 Channels</td>
</tr>
</tbody>
</table>
Figure 5-21 shows the experimental setup for the test and characterization of the accelerometers. Figure 5-22 shows one accelerometer chip under testing, where the test PCB is mounted on the shaker.

Figure 5-21. Photo of the test setup.

Figure 5-22. Test setup photo showing accelerometer under testing.
5.7 Experimental Results

5.7.1. DCA Self-Test

As shown in Figure 5-19, a replica of the DCA that is not connected to a sensor is used for the circuit characterization. In this case, the sensing capacitance $C_0$ is implemented with a fixed 150-fF poly-poly capacitor, and the self-test input signals are generated on a PC board. With a supply voltage $V_{DD}=3.3V$, it dissipates a current of 300 $\mu$A, resulting in a power consumption of 1 mW. In the test, $f_H$ is chosen as 1 MHz and $f_L$ is 20 kHz, and the modulation amplitude is 3.3 V. A load capacitor $C_L=1$ nF is used to remove the signals at the chopping frequency and its harmonics. Two chips were tested without the post-CMOS process to release the structure.

5.7.1.1 Frequency response and noise

Figure 5-23 shows the measured frequency response, where the DCA achieves a gain of 44.5 dB with a 3-dB bandwidth of 1.5 kHz.

Figure 5-23. Measured frequency response of the DCA.
Figure 5-24 shows the measured output noise spectrum of the DCA, which is $2.7 \mu V / \sqrt{Hz}$ at 20 Hz. Therefore the DCA achieves an input-referred noise of $16 \, nV / \sqrt{Hz}$.

![Figure 5-24. Measured output noise spectrum of the DCA.](image)

5.7.1.2 **Waveforms at various stages**

The operation of the DCA in the time domain is also tested. The output signals right before the second demodulator and the first demodulator were measured, with their waveforms shown in Figure 5-25. It is clear the signal right before the second demodulator is a square wave with frequency of $f_L=20$ kHz, while the signal waveform right before the first demodulator looks like a mixed clock. Figure 5-26 shows waveforms of both the test input and the output signal, where the test input is a 200-Hz, 10 mVpp sinusoidal signal generated on the test PCB board.
Figure 5-25. Measured waveforms. (a) Before the second demodulator. (b) Before the first demodulator.

Figure 5-26. Waveforms of test input and output with a 200-Hz, 10 mVpp input signal.
5.7.1.3 **DCA performance summary**

Table 5-2 summarizes the measured performance of the DCA prototype. With a 1 kHz bandwidth, the DCA achieves a capacitance resolution of 24 zF, which results in a charge resolution of $8 \times 10^{-20}$ Coulomb. In determining the capacitance resolution and charge resolution, the following relationships among electronic noise ($v_n$), bandwidth (BW), the minimum detectable voltage ($v_{min}$), the capacitance resolution (the minimum detectable capacitance change, $\Delta C_{min}$), and the charge resolution (the minimum detectable charge change, $\Delta Q_{min}$) are used.

\[ v_{min} = v_n \sqrt{BW} = \frac{\Delta C_{min}}{C_0} V_M \]  
\[ \Delta C_{min} = \frac{C_0 v_{min}}{V_M} = C_0 v_n \sqrt{BW} \]  
\[ \Delta Q_{min} = \Delta C_{min} V_M = C_0 v_n \sqrt{BW} \]

<table>
<thead>
<tr>
<th>Sensing Capacitance (4$\times$C$_0$)</th>
<th>4$\times$110 fF</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Chopping Clock</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Low Chopping Clock</td>
<td>20 kHz</td>
</tr>
<tr>
<td>Gain</td>
<td>44.5 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>1.5 kHz</td>
</tr>
<tr>
<td>Input-referred Noise</td>
<td>16 $nV / \sqrt{Hz}$</td>
</tr>
<tr>
<td>Circuit Residual Offset</td>
<td>$\leq$120 $\mu V$</td>
</tr>
<tr>
<td>Distortion (THD)</td>
<td>THD $&lt; 0.1%$ ($V_s \leq 2.2$ mVpp)</td>
</tr>
<tr>
<td></td>
<td>THD $&lt; 1%$ ($V_s \leq 17.3$ mVpp)</td>
</tr>
<tr>
<td>Capacitance Resolution</td>
<td>24 zF (BW=1kHz)</td>
</tr>
<tr>
<td>Charge Resolution</td>
<td>$8 \times 10^{-20}$ Coulomb</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1 mW</td>
</tr>
</tbody>
</table>
5.7.2. Single-Axis Accelerometer

In the single-axis accelerometer test, an on-board INA with a gain of 4 is used to convert the differential output voltage from the accelerometer into a single-ended signal.

5.7.2.1 Static test

Figure 5-27 plots the static response of the accelerometer in ±1 g acceleration range, showing a combined sensitivity of 229 mV/g, resulting in a 57.3 mV/g sensitivity from the accelerometer.

Figure 5-27. Static test results showing accelerometer output versus acceleration in –1 g to +1 g range. (a) With 0.1g per step. (b) With 2° per step.
5.7.2.2 Noise floor

For the dynamic tests, a reference accelerometer (KISTLER: 8638B5) with a sensitivity of 979 mV/g is mounted together with the tested accelerometer on the shaker table. The noise measurement was conducted using a shaker (LDS V-408) and the SRS-785 spectrum analyzer. The waveform and the spectrum of the accelerometer output in response to a 0.5-g, 50-Hz sinusoidal acceleration are shown in Figure 5-28 and Figure 5-29, respectively.

Figure 5-28. Output waveforms of the reference accelerometer and the tested accelerometer with 0.5-g, 50-Hz sinusoidal acceleration.

Figure 5-29. Output spectrum with 0.5-g, 50-Hz acceleration, RBW=0.25 Hz.
The accelerometer output noise spectrum is flat down to a few Hz, which means that the flicker noise in the interface circuit is completely removed. The measured noise from the output of the on-board INA is 11.9 $\mu V/\sqrt{Hz}$ at 20 Hz. Since the combined sensitivity is 229 mV/g, the accelerometer achieves a noise floor of 50 $\mu g/\sqrt{Hz}$. From the measured sensitivity and the DCA gain, the sensing element is found to have a transducer sensitivity of about 0.4 mV/g, which is much smaller than the designed value of 1 mV/g. The equivalent noise floor contributed by the interface circuits is about 40 $\mu g/\sqrt{Hz}$, while the thermalmechanical Brownian noise is about 30 $\mu g/\sqrt{Hz}$.

### 5.7.2.3 Performance summary

The measured performance of the single-axis accelerometer is summarized in Table 5-3. And Table 5-4 shows the comparison between simulation and measurements.

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>Sensing Capacitance ($4\times C_0$)</td>
<td>$4\times C_0$</td>
</tr>
<tr>
<td>Transducer Sensitivity</td>
<td>0.4 mV/g</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>57.3 mV/g</td>
</tr>
<tr>
<td>Noise Floor</td>
<td>50 $\mu g/\sqrt{Hz}$ @ 20 Hz</td>
</tr>
<tr>
<td>Brownian Noise</td>
<td>30 $\mu g/\sqrt{Hz}$</td>
</tr>
<tr>
<td>Equivalent Electronic Noise Floor</td>
<td>40 $\mu g/\sqrt{Hz}$</td>
</tr>
<tr>
<td>Linear Range</td>
<td>±8g (THD ≤3%)</td>
</tr>
<tr>
<td>Dynamic Range (BW = 100 Hz)</td>
<td>84 dB</td>
</tr>
<tr>
<td>Capacitance Resolution (BW = 100 Hz)</td>
<td>93 zF</td>
</tr>
<tr>
<td>Charge Resolution (BW = 100 Hz)</td>
<td>$3 \times 10^{-19}$ Coulomb</td>
</tr>
<tr>
<td>Displacement Resolution (BW = 100 Hz)</td>
<td>$2.48 \times 10^{-12}$ m</td>
</tr>
<tr>
<td>Force Resolution (BW = 100 Hz)</td>
<td>$6.16 \times 10^{-11}$ N</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1 mW</td>
</tr>
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Table 5-4. Comparison between design/simulation and test results

<table>
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<tr>
<th>Parameters</th>
<th>Design/Simulation</th>
<th>Measurements</th>
</tr>
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<tbody>
<tr>
<td>Sensing Capacitance (4×C₀)</td>
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<td>4×110 fF</td>
</tr>
<tr>
<td>Transducer Sensitivity</td>
<td>1 mV/g</td>
<td>0.4 mV/g</td>
</tr>
<tr>
<td>Brownian Noise</td>
<td>20 μg/√Hz</td>
<td>30 μg/√Hz</td>
</tr>
<tr>
<td>Electronic Noise</td>
<td>15 nV/√Hz</td>
<td>16 nV/√Hz</td>
</tr>
<tr>
<td>Equivalent Electronic Noise Floor</td>
<td>15 μg/√Hz</td>
<td>40 μg/√Hz</td>
</tr>
<tr>
<td>Noise Floor</td>
<td>25 μg/√Hz</td>
<td>50 μg/√Hz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1 mW</td>
<td>1 mW</td>
</tr>
</tbody>
</table>

5.7.2.4 Temperature sensitivity

Temperature sensitivity of the single-axis accelerometer is also measured with the accelerometer heated by a thin-film heater. With zero acceleration, Figure 5-30 shows the accelerometer output drift within temperature range between 20ºC to 100ºC. An output drift of 7 mg/ºC is observed. Figure 5-31 shows the accelerometer sensitivity change in the same temperature range. With the sensitivity normalized to the value measured at room temperature (20ºC), the maximum sensitivity variation is measured as 23%.

Figure 5-30. Measured output drift with temperature variation.
The accelerometer sensitivity variation and output drift resulted from temperature change are mainly due to the temperature sensitivity of the open-loop implementations of the first stage $A_1$ and the low-pass filter (LPF) in the DCA interface circuit. In the implementations of $A_1$ and LPF, diode-connected NMOS transistors are used as the active load and the input pairs are PMOS transistors. Temperature sensitivity in these circuits comes from the different temperature coefficients of the mobilities of electrons and holes. Temperature-insensitive $A_1$ and LPF are shown in Figure 5-32, where the active loads are diode-connected PMOS transistors. To the first order, the gain of these circuits is only determined by biasing current and the transistor geometry ratios. For instance, the small signal gain of $A_1$ implemented in Figure 5-32(a) is given by:

$$\frac{A_v}{g_m} = \frac{g_m (1,2)}{g_m (3,4)} = \sqrt{\frac{I_{D (1,2)}}{I_{D (3,4)}}} \left( \frac{W}{L} \right)_{(1,2)} \left( \frac{W}{L} \right)_{(3,4)}$$

(5.11)
Figure 5-32. Temperature-insensitive implementation of $A_1$ and LPF.
The temperature insensitivity of these improved implementations can be easily verified. Figure 5-33 shows the simulated results of the new implementation of A1, in which, the gain variation of A1 is about 1-2% in the temperature range from 0 to 100 °C. In practical implementations, a gain accuracy of about 1-2% can be achieved. It is well below the sensitivity accuracy of the overall MEMS accelerometers, which is normally about 5% to 10%.

![Figure 5-33. Simulation results of new implementation of A1](image)

### 5.7.3. 3-Axis Accelerometer

Due to the large size of the X and Y-axis sensing elements in the 3-axis accelerometer, a modulation amplitude of 1 V is applied to these lateral accelerometers.

#### 5.7.3.1 Static test

The sensitivities of the lateral-axis and z-axis accelerometers were measured as 560 mV/g and 320 mV/g, respectively. A Piezotronics shaker providing 1-g acceleration at 159.1 Hz is used in the characterization. Figure 5-34 shows the static test results of the lateral and vertical axes.
Due to the asymmetry of the z-axis proof mass, the cross talks of the z-axis sensing were measured to be 2.1% from x-axis and 4.7% from y-axis, respectively.

5.7.3.2 Noise floor

The spectral response of the Z-axis output under a 0.5-g, 200-Hz acceleration is shown in Figure 5-35. The overall noise floor of the Z-axis accelerometer is measured as $110 \ \mu g / \sqrt{Hz}$ at 200 Hz. Both X and Y-axis sensing elements have the same sensitivity due to the symmetric mechanical and electrical design. The spectrum of the Y-axis output under a 200-Hz, 0.05-g acceleration is shown in Figure 5-36, where an overall noise floor of $12 \ \mu g / \sqrt{Hz}$ at 200 Hz is demonstrated. The various frequency components shown in the spectrum are due to the mechanical modes from the mounting PCB board.
Figure 5-35. The spectrum of the z-axis output with a 0.5-g, 200-Hz sinusoidal acceleration (RBW = 1Hz).

Figure 5-36. The spectrum of the y-axis accelerometer output with a 0.05-g, 200-Hz sinusoidal acceleration (RBW = 1Hz).
5.7.3.3 Performance summary

The measured performance specifications of the integrated 3-axis accelerometer are summarized in Table 5-5.

Table 5-5. Performance summary of the 3-axis accelerometer

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size</td>
<td>3 mm × 3 mm</td>
</tr>
<tr>
<td>Sensitivity in Lateral Axes</td>
<td>560 mV/g</td>
</tr>
<tr>
<td>Sensitivity in Z-axis</td>
<td>320 mV/g</td>
</tr>
<tr>
<td>Circuit Input-Referred Noise</td>
<td>16 nV/√Hz</td>
</tr>
<tr>
<td>Noise Floor of Lateral Axes</td>
<td>12 μg/√Hz</td>
</tr>
<tr>
<td>Noise Floor of Z-Axis</td>
<td>110 μg/√Hz</td>
</tr>
<tr>
<td>Power Dissipation/Axis</td>
<td>1 mW</td>
</tr>
</tbody>
</table>

5.7.4 Comparison to Previous Work

Table 5-6 compares the integrated single-axis and 3-axis accelerometers in this work to previously reported capacitive MEMS accelerometers. Among monolithic integrated accelerometers using CMOS interface circuits, both the lowest noise floor and the lowest power consumption are achieved in this work.

From the system point of view, the single-axis accelerometer is close to the optimal design, since the equivalent noise contributed by the interface circuit is comparable to the Brownian noise floor, which is about 20-30 μg/√Hz.

For the lateral axes in the 3-axis accelerometer, the DCA interface circuits are a little over-designed. This is due to the fact that the lateral axes have much larger size and larger transducer sensitivity than the single-axis accelerometer. With the DCA interface
circuits, an optimally designed lateral axis accelerometers could achieve a resolution at the level of μg.

Table 5-6. Comparison of capacitive accelerometers in noise floors and power

<table>
<thead>
<tr>
<th>MEMS Technology</th>
<th>Interface Technology</th>
<th>Noise floor (μg/√Hz)</th>
<th>Power dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly surface, monolithic</td>
<td>Switched-capacitor</td>
<td>110</td>
<td>45 mW</td>
</tr>
<tr>
<td>CMOS-MEMS, monolithic</td>
<td>Chopper-stabilization</td>
<td>50</td>
<td>30 mW</td>
</tr>
<tr>
<td>SCS bulk + ASIC</td>
<td>Switched-capacitor</td>
<td>15</td>
<td>6.6 mW</td>
</tr>
<tr>
<td>SOI + ASIC</td>
<td>Switched-capacitor</td>
<td>110</td>
<td>6 mW</td>
</tr>
<tr>
<td>Poly surface, monolithic</td>
<td>Chopper-stabilization</td>
<td>110</td>
<td>3.5 mW</td>
</tr>
<tr>
<td>2 poly surface +ASIC, hybrid</td>
<td>Switched-capacitor</td>
<td>350</td>
<td>1.7 mW</td>
</tr>
<tr>
<td>SCS + ASIC, hybrid</td>
<td>Switched-capacitor</td>
<td>175</td>
<td>2.2 mW</td>
</tr>
<tr>
<td>BiCMOS, hybrid</td>
<td>Switched-capacitor</td>
<td>50</td>
<td>3.3 mW</td>
</tr>
<tr>
<td>DRIE CMOS-MEMS</td>
<td>CTV with DCA</td>
<td>50</td>
<td>1 mW</td>
</tr>
<tr>
<td>DRIE CMOS-MEMS</td>
<td>CTV with DCA</td>
<td>12</td>
<td>1 mW/axis</td>
</tr>
</tbody>
</table>

5.8 Summary

This chapter describes the detailed design and test results of the DCA circuit for monolithic capacitive CMOS-MEMS accelerometers. Its ability to achieve both low noise and low consumption has been successfully demonstrated with experimental results of the integrated single-axis and 3-axis accelerometers.
CHAPTER 6
LOW-NOISE LOW-POWER CAPACITIVE AMPLIFIER FOR CORIOLIS ACCELERATION SENSING IN CMOS-MEMS GYROSCOPES

In this chapter, a new open-loop, two-stage chopper amplifier for Coriolis acceleration sensing in CMOS-MEMS gyroscopes is designed and tested. By utilizing an active mixer as the demodulator, it achieves low noise level in the Coriolis acceleration range (~15 kHz) with low power consumption (1 mW). In implementation, the active mixer is embedded in a folded-cascode amplifier with a linearized trans-conductance load, in which low-impedance-node chopping (LINC) and dynamic element matching (DEM) are utilized to allow high chopping frequencies.

5.1 Operation Principle of Vibratory Gyroscopes

Vibratory gyroscopes determine rotation rate by vibrating a proof mass and measuring Coriolis acceleration. The operation of a Z-axis vibratory gyroscope is illustrated in Figure 6-1. The proof mass is driven into oscillation along the Y-axis (the drive mode). The rotation around the Z-axis causes the proof mass to experience the induced Coriolis acceleration along the X-axis, consequently resulting in an oscillatory motion (the sense mode) along the X-axis [1, 14].

The Coriolis acceleration ($\vec{a}_c$) is proportional to the vibration velocity ($\vec{V}$) in drive mode and the imposed rotation rate ($\dot{\Omega}$), i.e.:

$$\vec{a}_c = 2\vec{V} \times \dot{\Omega}$$  \hspace{1cm} (6.1)
It is obvious that $\ddot{a}_c$ can be considered as $\ddot{\Omega}$ modulated by the vibrating velocity $\dot{V}$.

The final value of $\ddot{\Omega}$ is recovered when $\ddot{a}_c$ is demodulated with the vibrating velocity signal. In most applications, $\ddot{\Omega}$ has a bandwidth of several Hz to tens of Hz, and $\ddot{a}_c$ has a frequency from several kHz to 20 kHz [14].

Capacitive sensing is the dominant mechanism in MEMS gyroscopes, but in monolithic MEMS gyroscopes, both the sensing capacitance and the mechanical sensitivity from sensing element are extremely small. For instance, in the DRIE CMOS-MEMS gyroscope reported in [25], the sensing capacitance is only 0.1 pF, and the sensed Coriolis acceleration from the transducer results in a voltage signal of 0.1 $\mu$V to 1 mV for a rotation signal with a 100 Hz bandwidth and a $\pm 300^\circ$/s input range. Therefore, achieving very low electronic noise is the primary target in the readout circuit design in
monolithic MEMS gyroscopes. Bipolar transistors, which have a very low flicker noise corner, have been utilized in the signal path for Coriolis acceleration sensing in [19], where a BiCMOS process is used. For gyroscopes integrated on pure CMOS processes, low-frequency flicker noise must be effectively removed or reduced in the readout circuits. However, most reported designs have a power dissipation of a few tens of mWs, which greatly limits their applications in portable and wireless products requiring long lifetime operation [30].

5.2 Low-Noise Low-Power Chopper Amplifier Architecture

We proposed a two-stage continuous-time chopper amplifier to amplify the Coriolis acceleration signal in CMOS-MEMS gyroscopes, which can achieve both low noise and low power dissipation simultaneously. In addition, this architecture also offers a good balance among other performance specifications such as gain, linearity, signal swing, circuit offset and sensor offset cancellation.

Figure 6-2 shows the architecture diagram of the proposed readout circuit. A full capacitive bridge is formed by the mechanical sensing capacitors provided by the sensing structure. The complementary modulation clocks (with frequency $f_M \geq 1$ MHz) are applied to the outer plates of the capacitive bridge. The Coriolis acceleration modulated at $f_M$ is applied to the inputs of the readout circuit. To satisfy the requirements of both low noise and low power consumption, the first amplification stage, $A_1$, is implemented in an open-loop configuration. This is partially benefited from the metal wiring enabled by the DRIE CMOS-MEMS technology. The input-referred noise of $A_1$ is minimized with the optimal-sizing technique introduced in section 3.1.2. Without sacrificing the noise performance of $A_1$, a moderate gain (about 10) can also be achieved from this stage, so that the noise from following stages can be less significant.
Figure 6-2. Architecture diagram of the proposed 2-stage, continuous-time chopper amplifier readout circuit.

The sensed Coriolis acceleration signal from the sensing element is extremely low, so very large gain is required from the readout circuit to boost the signal level. For instance, in [19], a total gain of about 2500 is provided in the sensing path. In order to avoid large power consumption with a high chopping frequency, this new architecture converts the signal back to the baseband right after the amplification of $A_1$. Then, one major part of the gain can be offered by the second amplification stage, $A_2$, which boosts the signal in the baseband (Coriolis acceleration frequency) with a much smaller gain-bandwidth requirement. Therefore, the power consumption in this stage can be greatly reduced. The input transistor pair of $A_2$ can have a much larger size compared to that of $A_1$, so its flicker noise corner can be easily made below the Coriolis acceleration frequency range ($1\text{kHz} \sim 20\text{kHz}$). In addition, either open-loop or close-loop configuration can be used for $A_2$, depending on the trade-off among gain, noise, power,
linearity and output signal swing. The sensor offset can be tuned with the two auxiliary inputs \( V_{os+} \) and \( V_{os-} \) of stage \( A_2 \).

The large circuit offset from \( A_1 \) resulted from its small input transistor size is removed by ac coupling. Otherwise, a high-order low-pass filter is needed after the demodulation to effectively remove the large signals at the chopping clock frequency and its harmonics. Low power dissipation of the demodulation and low-pass filter block is achieved with the active mixer demodulation technique described in the following section.

5.3 Low-Power Active-Mixer Demodulator

5.3.1 Chopping Frequency Limitation in Passive Chopper Amplifier

Traditionally, chopper amplifiers utilize the four-switch chopper (passive mixer) for signal modulation and demodulation, as shown in Figure 6-3. When used in voltage signal switching, a passive chopper is known for its high linearity and non-power dissipation. However, its ability to support high chopping frequency is very limited, because the finite output impedance of the amplification stage before the demodulation chopper, and the capacitive load \( C_1 \) in Figure 6-3) following the chopper results in signal loss at high chopping clock frequency. This signal loss effect is illustrated in Figure 6-3(b), where \( r_o \) is the output resistance of the amplifier \( A \), and the equivalent input resistance \( R_{eq} \) to the demodulation chopper is resulted from capacitive load \( C_I \) in Figure 6-3(a). Since the signal is modulated at the chopping frequency before the demodulation, \( Z_{eq} \) can be estimated as [37]:

\[
Z_{eq} = \frac{T}{2C_1} \tag{6.2}
\]

where \( T \) is \( 1/f_M \), the period of the chopping clock.
The signal loss is due to the voltage divider formed by $r_o$ and $Z_{eq}$. To make the signal loss negligible, $r_o$ is required to be much smaller than $Z_{eq}$.

From another point of view, the capacitive load to the demodulation chopper, $C_1$, limits the bandwidth of the amplification stage before the demodulation, where the signal needs to be amplified at the high frequency band (the chopping frequency). To reduce the load effect of $C_1$, the pole formed by $r_o$ and $C_1$ must have a frequency much higher than the chopping frequency $f_M$, i.e.,

$$f_{pole} = \frac{1}{2\pi r_o C_1} >> f_M \quad (6.3)$$

In real circuit implementations, the amplifier must have a low output impedance, which normally is provided by a voltage buffer. Since $r_o$ is about $1/g_m$, a large chopping
frequency $f_M$ consequently requires large $g_m$, resulting in large power dissipation for the readout circuit.

### 5.3.2 High Chopping Frequency Ability in Active Mixer

One natural choice for high frequency modulation/demodulation is the active mixer, which is widely used in radio frequency (RF) circuits for frequency conversion [45-47]. The active mixer topology shown in Figure 6-4(a) is applied for the signal demodulation and low-pass filtering block of the low-power readout circuit shown in Figure 6-2. It is a double-balanced active mixer with low-impedance-node chopping (LINC). In active mixers, the signal demodulation is carried out in the current mode, and its ability to support high chopping clock frequencies is shown in Figure 6-4(b). The parasitic capacitance after the chopper ($C_1$ in Figure 6-4(a)) and the resistance from node XX’ form a pole with a frequency of:

$$f_p = \frac{g_{m(3,4)}}{2\pi C_1}$$

Since at node X and X’, the signal current has already been converted into the baseband, which has a frequency ($f_{\text{Coriolis}}$) in 10 kHz range for the Coriolis acceleration signal. As long as $f_p$ is much larger than $f_{\text{Coriolis}}$, the demodulation will introduce little signal loss. Cascode transistors M3 and M4 act as current buffer, and the capacitive load $C_L$ has little effect on the conversion gain, since the pole formed by $R_L$ and $C_L$ only influence the demodulated signal at the baseband. In practice, $f_{\text{Coriolis}}$ is about 1/100 of the $f_M$, and $f_p$ can be chosen a value close to $f_M$ or even much lower. Therefore the $g_{m(3,4)}$ can be made much smaller and very low power dissipation is needed for the demodulation.
Figure 6-4. Active mixer with LINC for demodulation. (a) Schematic. (b) Model showing its high frequency capability.

The comparison of the passive chopper demodulation and the active mixer demodulation at high chopping frequency is shown in Figure 6-5. The X-axis is the 3-dB frequency \( \frac{g_m}{C_1} \) normalized to the chopping frequency. For the passive chopper, it is obvious that the chopping frequency must be about 10 times lower than the effective pole frequency to avoid signal attenuation, while for the active mixer the chopping frequency can be 10 times higher than the pole frequency without introducing significant signal loss.
Another advantage of this active mixer demodulation topology is that the signal is converted from current to voltage at the base band, the low-pass filter formed by the load resistance $R_L$ and capacitance $C_L$ further reduces high frequency power at the chopping frequency and its harmonics due to the finite circuit bandwidth and circuit offset.

A third advantage of the active mixer over the passive chopper is that it can provide extra gain, while the latter always introduce some signal loss depending on the amplifier bandwidth and other non-idealities. However, since the dc offset of the active mixer will be modulated to the chopping frequency after the signal being demodulated, normally a
low gain is required for the active mixer to ease the design of the following low-pass filter.

5.3.3 Flicker Noise in Active Mixer

When used to switch voltage signals, passive choppers contribute no flicker noise since they operate in the linear region with no dc current. In the active mixer topology since non-overlap clocks are used to control the PMOS choppers, there is some finite time in each chopping clock period when both current paths are on, as illustrated in Figure 6-5(a). It is well studied that during the both-on time the flicker noise of the trans-conductance input transistor pair will leak to the output and contaminate the base signal. A qualitative solution to this noise leakage problem is suggested in [46], which is to make the both-on time as small as possible and make the transition sharp.

Since an active mixer is a time variant system, analytical analysis of the flicker noise leakage problem is tedious and impractical. Nevertheless, it can be estimated with Periodic Steady State (PSS) analysis from SpectreRF provided by Cadence. Simulated results of flicker noise leakage with different both-on times and different chopping frequencies are shown in Figure 6-6(b) and 6-6(c), respectively. Figure 6-6(b) shows that with 1 MHz chopping clock frequency, the flicker noise corner of the active mixer is about 1 kHz, even though the both-on time is as large as 10 ns. Figure 6-6(c) shows the relation between the flicker noise corner and the chopping frequency, with a fixed both-on time of 10 ns. In this case, the active mixer still has a flicker noise corner below the Coriolis acceleration frequency (10 kHz) when the clock frequency is up to 8 MHz. In today’s submicron technology, the both-on time of the chopping clocks can be easily made below 2 ns, so the active mixer block contributes negligible flicker noise to the signal.
Figure 6-6. Flicker noise in active mixer demodulator. (a) Non-overlap clock used to control the PMOS chopper. (b) Noise versus both-on time with chopping frequency of 1 MHz. (c) Noise versus chopping frequency with fixed both-on time of 10 ns.
The prototype of this design is implemented in TSMC 0.18 μm process with thick oxide to allow a 3.3V power supply.

5.4 Prototype Circuit Design

5.4.1 Design of High-Bandwidth Amplifier A₁

The schematic of the first stage is shown in Figure 6-7. M₁ and M₂ form the PMOS input pair with optimal sizes to achieve the minimum noise with respect to the sensing and parasitic capacitance at the sensing nodes. M₃ and M₄ are cascoded transistors to reduce the Miller effect, which will attenuate the effective gain otherwise. A combination of diode-connected transistors (M₅, M₆) and current sources (M₇, M₈) is used as the active load. A moderate gain about 10 is obtained to effectively reduce the noise from the following stages. With a 120μA current dissipation, it achieves gain of 10 and a 3-dB bandwidth of 10 MHz.

Figure 6-7. Schematic of amplifier A₁.
5.4.2 Design of Low-Bandwidth Amplifier/Active Mixer A₂

The first stage is ac coupled to the second stage whose dc bias is also obtained through the MOS-Bipolar devices. The schematic of the second stage is shown in Figure 6-8, where low-impedance-node chopping (LINC) and dynamic element matching (DEM) are used. It is basically a folded-cascode amplifier with a linearized transimpedance load if the LINC and DEM are not considered. This can be seen in the schematic if the dashed lines are connected and the two choppers are removed. The LINC and the DEM are implemented in a fully differential way. As shown in the schematic, the N-chopper, which consists of four NMOS switches, is used to chop the signal at the low impedance nodes. The P-chopper, which comprises four PMOS switches, is used for dynamic element matching (DEM) of M₁₁ and M₁₂. With DEM, the average currents through M₁₁ and M₁₂ will be exactly equal, and their flicker noise currents will be chopped to a high frequency. The overlapped 2-phase clocks are applied to these both the N- and P-choppers to ensure a stable dc sink currents. With this topology, the flicker noise of all transistors, except M₁₃-M₁₆, are effectively removed. Because the signal has already been converted to the base band at the output nodes, the size of M₁₃-M₁₆ can be made large to reduce their flicker noise. At the same time, the dc offset of this stage has been chopped to a high frequency and then low-passed at the output nodes. Therefore, no extra circuitry for the dc offset cancellation is needed. This stage dissipates 180 μA current, and it provides a conversion gain of 20 at the Coriolis acceleration band.
5.5 Experimental Results

The self-test prototype circuit with 1 pF sensing capacitance is implemented and fabricated using the TSMC 0.18μm 6-Metal process through MOSIS. The thick oxide option is chosen to allow 3.3V power supply. The block diagram and layout of the prototype circuit are shown in Figure 6-9(a) and 6-9(b), respectively, where the circuit layout has a size of 300 μm×600μm. The chip photograph is shown in Figure 6-10.
Figure 6-9. Prototype circuit implementation. (a) Block diagram. (b) Layout.

Figure 6-10. Chip photo.
An evaluation PCB board is made to test the circuit. An instrumentation amplifier (INA 122P) is used on-board to provide the differential-to-single-ended conversion, and it also provides an accurate gain of 5. A 1 MHz chopping clock is used in the test. Small test signals generated on the PCB board are applied to the test chip. Figure 6-11(a) shows a 10 kHz, 6 mVp-p test input signal captured through Labview. Figure 6-11(b) shows a 3 Vpp from the output of the instrumentation amplifier, resulting in a 600 mVpp at the final-stage output of the on-chip circuit. Thus, a gain of 100 is achieved from the on-chip interface amplifier.

Figure 6-11. Waveforms of test signal. (a) 6 mVpp test input. (b) 3 Vpp at the INA output.
As shown in Figure 6-12(a), with a 6 mVpp test input, the amplifier achieves a gain of 40 dB with a 3-dB bandwidth up to 50 kHz, which is limited by the output buffers and load capacitance. At the test frequency of 10 kHz, when the input signal level is increased to 30 mVp-p, a value that is much higher than the maximum sensed Coriolis signal, the gain of the amplifier drops by 2.6 dB, as shown in Figure 6-12(b). The measured output noise spectrum with different chopping clock frequencies are shown in Figure 6-13.

Figure 6-12. Measured frequency response and linearity. (a) Gain versus frequency. (b) Gain versus input signal level.
Figure 6-13. Spectrum of output noise with different chopping frequency.

No chopping

- $16.32 \mu V/\sqrt{Hz}$ at 2 kHz
- $2.266 \mu V/\sqrt{Hz}$ at 2 kHz
- $1.981 \mu V/\sqrt{Hz}$ at 2 kHz
- $1.864 \mu V/\sqrt{Hz}$ at 2 kHz
It is clear that the flicker noise is effectively removed when the chopping frequency is 1 MHz and above. With 1 MHz chopping clock frequency, the amplifier achieves an equivalent input noise level of $20 \, nV/\sqrt{Hz}$ in the frequency range between 1 kHz to 20 kHz. Noise tests also show that the flicker corner of this chopper amplifier is reduced to about 100 Hz, which is much lower than the frequency of Coriolis acceleration signal. To minimize both the noise level and power dissipation, the optimal chopping clock frequency should be around 1 MHz. The residual flicker noise at very low frequency is due to the fact that the flicker noise from transistors M13-M16 can not be completely cancelled. The dc offset from the output of the tested amplifier is 20 mV, which corresponds to an equivalent input offset of less than 200μV. The tested results of the low noise, low power amplifiers are summarized in table 5-1.

<table>
<thead>
<tr>
<th>Sensing capacitance</th>
<th>1 pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chopping clock frequency</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Gain</td>
<td>40 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>16 kHz</td>
</tr>
<tr>
<td>Input-referred noise</td>
<td>$20 , nV/\sqrt{Hz}$</td>
</tr>
<tr>
<td>Circuit residual offset</td>
<td>$\leq200 , \mu V$</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1 mW</td>
</tr>
</tbody>
</table>

**5.6 Discussion**

The active mixer demodulator can achieve low noise and low power consumption simultaneously. However, it has poorer linearity than the passive chopper counterpart. One of the solutions to obtain better linearity is to consume more power. In addition, the
active mixer itself has offset, which is converted to a high frequency signal after the
demodulation. To avoid complex low-pass filter design after the demodulation, normally
a low conversion gain (less than 10 dB) is desirable for the active mixer. Another
drawback of the chopper-amplifier with LINC and DEM is its open-loop configuration,
which has worse performance in gain accuracy, linearity, and temperature sensitivity than
close-loop configurations.

In MEMS gyroscopes, high gain is generally needed in the sensing path due to the
everribly small Coriolis acceleration signal. The architecture discussed in this chapter
can easily satisfy this high gain requirement without consuming too much power. As
shown in Figure 6-2, the basband amplification stage $A_2$ can further boost the Coriolis
acceleration signal before it is finally demodulated with the driving signal. And both the
noise and the power dissipation of $A_2$ are not a big concern.

5.7 Summary

A low noise, low power chopper amplifier for Coriolis acceleration sensing in the
integrated CMOS-MEMS gyroscope is implemented, fabricated and tested. Test results
show that the optimal chopping frequency for this architecture is about 1 MHz. When
chopped at 1 MHz, the amplifier achieves a gain of 40 dB in the Coriolis signal band, and
a noise floor of $20 \, nV / \sqrt{Hz}$ within the frequency range from 1 kHz to 20 kHz. It is also
shown that the amplifier maintains good linearity up to 30 mVp-p input signal level,
which is much higher than the maximum Coriolis signal from the transducer. Finally,
with a 3.3 V supply voltage, the amplifier consumes a power of 1 mW.
CHAPTER 7
CONCLUSIONS AND FUTURE WORK

In this work, capacitive sensing circuit techniques that achieve both low noise and low power consumption are investigated to realize low-power and high-performance integrated CMOS-MEMS accelerometers and gyroscopes. Two novel readout circuits have been designed, tested and applied to a single-axis and a 3-axis accelerometer.

6.1 Summary of Results

In the area of interface circuits for MEMS inertial sensors, we investigated the fundamental limits on low-noise and low-power design for capacitive sensing. To overcome the performance constraints of continuous-time voltage sensing based on conventional chopper amplifiers, we proposed the novel dual-chopper amplifier (DCA) architecture for capacitive CMOS-MEMS inertial sensors to achieve both low noise and low power dissipation simultaneously. We also demonstrated that the active-mixer topology can be used as the demodulator and low-pass filtering block in the sensing path for the Coriolis acceleration in vibratory gyroscopes. We introduced the MOS-Bipolar pseudoresistor technique for stable biasing of the high-impedance sensing nodes in continuous-time capacitive sensing. The DCA prototype achieves an input-referred noise of $16 \text{nV/}\sqrt{\text{Hz}}$ at low frequency down to dc. An integrated single-axis CMOS-MEMS accelerometer prototype using these techniques achieves $50 \text{\mu g/}\sqrt{\text{Hz}}$ with 1 mV power dissipation. With a 100-Hz bandwidth for the acceleration signal, the accelerometer offers a dynamic range of 84 dB. In addition, a 3-axis CMOS-MEMS accelerometer
utilizing these circuit techniques achieves a noise floor of $12 \, \mu g / \sqrt{Hz}$ for X and Y-axis, and the Z-axis for $110 \, \mu g / \sqrt{Hz}$ noise floor.

6.2 Suggestions for Future Work

The ultimate goal of the research on integrated MEMS inertial sensors is to produce monolithic inertial measurement units (IMU) with 6 degree-of-freedom (DOF) sensing capability. As shown in Figure 7-1, an ideal IMU should have 3-axis accelerometers, 3-axis gyroscopes and the interface and signaling circuitry all integrated on a single chip. In addition, it needs to have advanced features such as providing digital outputs and/or wireless communication. The design challenges of the integration issues of 6-DOF MEMS IMU and the circuitry for wireless communication are not discussed here. I mainly focus on research opportunities and design improvements in the interface and signal-conditioning circuitry block. Generally this block comprises of three major parts as follows:

- a. Capacitive readout circuits
- b. Interface circuits such as analog-to-digital conversion (ADC) and PWM
- c. Control and actuation circuits such as $\Sigma-$Δ force feedback and driving circuits for vibratory gyroscopes.
Following the work presented in this dissertation, the future improvements in interface circuits design for CMOS-MEMS accelerometers and gyroscopes may include:

1. Designing temperature-insensitive building blocks that can be used with the open-loop configuration in the DCA;
2. Designing on-chip band-gap reference circuitry to generate temperature-insensitive reference voltages and currents;
3. Designing on-chip clock generation circuitry (e.g. relaxation-time clock circuit); and
4. Adding circuits with which the overall sensitivity and sensor offset can be digitally tuned.

In real applications, low-cost, high-performance accelerometers and gyroscopes with digital outputs are highly desired. In designs with digital outputs, oversampling $\Sigma$-$\Delta$ A/D converters are generally required, so that the quantization noise can be made comparable or even lower than the Brownian noise and interface circuit noise level.

With the DRIE CMOS-MEMS technology, when the Brownian noise is brought down to the $\mu g / \sqrt{Hz}$ level, the overall noise performance will once again be dominated by the circuit noise. The possible solutions to reduce the equivalent noise contributed by the interface circuits in this case are:

(a) To increase mechanical sensitivity from the sensing element;

(b) To increase the sensing capacitance so that large input transistors can be used in the interface circuit to reduce $1/f$ noise; and

(c) To increase the power consumption of the interface circuits, since thermal noise is the fundamental limit and is inversely proportional to the power. However, this will limit the potential applications of MEMS inertial sensors in portable and wireless applications.

6.3 Technology Directions

Advancements in both MEMS processing and interface circuit technologies will undoubtedly bring MEMS inertial sensors with small size, low cost, low power and high performance into the market. The low-noise low-power interface techniques introduced in this work may become increasingly important in the future in the MEMS inertial sensors industry.
APPENDIX A
MECHANICAL SENSING PRINCIPLE OF ACCELEROMETER

A.1 Mechanical Sensing Principle

In MEMS accelerometers, acceleration measurement is achieved by a proof-mass, spring and damper system made up of microfabricated structures. A lumped-element model of the system is shown in Figure A-1.

The substrate acceleration generates an inertial force on the proof-mass, which is anchored to the substrate with springs. The inertial force then results in the displacement of the proof-mass. In the operation range of the accelerometer, the spring elastic force is linear with the displacement, and the viscous damping force is linear with the proof-mass velocity. Therefore, the differential equation in sensing axis is given by:

\[ F_{in}(t) = ma_{in}(t) = m\ddot{x}(t) + b\dot{x}(t) + kx(t) \] (A.1)

where \(m\) is the proofmass, \(b\) is the damping coefficient and \(k\) is the spring constant.

The natural resonance frequency \(\omega_0\) is defined as:

\[ \omega_0 = \sqrt{\frac{k}{m}} \] (A.2)

And the mechanical quality factor \(Q\) is defined as:

\[ Q = \sqrt{\frac{km}{m\omega_0}} = \frac{m\omega_0}{b} \] (A.3)

Then, the differential equation can be rewritten as:

\[ a_{in}(t) = \frac{F_{in}(t)}{m} = \ddot{x}(t) + \frac{\omega_0}{Q} \dot{x}(t) + \omega_0^2 x(t) \] (A.4)
A device is under-damped if Q>0.5, critically damped if Q=0.5, and over-damped if Q<0.5. At frequencies much lower than the resonant frequency, the sensitivity of the accelerometer is given by:

\[ S_T = \frac{x}{a_{in}} = \frac{m}{k} = \frac{1}{\omega_0^2} \]  

(A.5)

It is clear that in the accelerometer structure design, there is a tradeoff between bandwidth and sensitivity with respect to the resonant frequency \( \omega_0 \).

When the Laplace transformation is used, the differential equation can be transformed into the s-domain. The transfer function of the accelerometer is:

\[ T(s) = \frac{X(s)}{A_{in}(s)} = \frac{1}{s^2 + \frac{\sigma_b}{Q}s + \sigma_0^2} \]  

(A.6)

**A.2 Damping and Brownian Noise**

There are two sources of mechanical damping: the structure damping and the viscous damping by gas flows. The DRIE CMOS-MEMS structures are made of single-crystal silicon and CMOS layers (Aluminum and SiO₂), and both are high-Q materials.
with very low structural damping. Therefore, the squeeze-film damping between parallel-plate capacitor fingers is the dominant damping mechanism, which is approximately given by:

$$b \propto \mu_{\text{eff}} h \left( \frac{l}{d} \right)^3$$  \hspace{1cm} (A.7)

where \(l\) and \(h\) are the length and the thickness of the fingers, \(d\) is the distance between the fingers, and \(\mu_{\text{eff}}\) is the effective viscosity of the gas.

A direct consequence of air damping is the thermal-mechanical noise, which is a random force generated by the Brownian motion of the ambient molecules. And this is normally called Brownian noise. The power spectral density (PSD) of the Brownian noise force is given by:

$$F_n^2(f) = 4kTb \quad \text{N}^2/\text{Hz} \quad (A.8)$$

where \(b\) is the mechanical damping coefficient.

For accelerometers, the PSD of the input-referred Brownian noise is:

$$a_{nn}^2(f) = \frac{4kTb}{9.8^2 m^3} \quad \text{g}^2/\text{Hz} \quad (A.9)$$

and the input-referred Brownian noise floor is:

$$a_{nn}(f) = \frac{\sqrt{4kTb}}{9.8m} \quad \text{g}/\sqrt{\text{Hz}} \quad (A.10)$$

In surface micromachined accelerometers, \(a_{nn}\) is above tens of \(\mu g/\sqrt{\text{Hz}}\); while in bulk micromachined accelerometers, \(a_{nn}\) can be sub- \(\mu g/\sqrt{\text{Hz}}\).
APPENDIX B
SENSING ELEMENTS OF 1-AXIS AND 3-AXIS ACCELEROMETERS

The dimensions of the structures in the 1-axis accelerometer are listed in Table B-1.

Table B-1. Structural dimensions of the designed single-axis accelerometer

<table>
<thead>
<tr>
<th>Parts (unit)</th>
<th>Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proof mass area</td>
<td>300μm × 600μm</td>
</tr>
<tr>
<td>Length of single turn spring (μm)</td>
<td>200</td>
</tr>
<tr>
<td>Width of single turn spring (μm)</td>
<td>4</td>
</tr>
<tr>
<td>Length of meander (μm)</td>
<td>13</td>
</tr>
<tr>
<td>Width of meander (μm)</td>
<td>10</td>
</tr>
<tr>
<td>Length of comb finger (μm)</td>
<td>85</td>
</tr>
<tr>
<td>Length of effective comb finger (μm)</td>
<td>80</td>
</tr>
<tr>
<td>Width of comb fingers (μm)</td>
<td>4.8</td>
</tr>
<tr>
<td>Gap of the fingers (μm)</td>
<td>4</td>
</tr>
<tr>
<td>Thickness of all the structure (μm)</td>
<td>37</td>
</tr>
</tbody>
</table>

The dimensions of the structures in the 3-axis accelerometer are listed in Table B-2.

Table B-2. Structural dimensions of the designed 3-axis accelerometer

<table>
<thead>
<tr>
<th>Structures</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral proof mass (μm×μm)</td>
<td>900 × 900</td>
</tr>
<tr>
<td>Torsional plate (μm×μm)</td>
<td>500 × 300</td>
</tr>
<tr>
<td>Structure Thickness (μm)</td>
<td>50</td>
</tr>
<tr>
<td>Lateral sensing finger length (μm)</td>
<td>80</td>
</tr>
<tr>
<td>Z sensing fingers length (μm)</td>
<td>50</td>
</tr>
<tr>
<td>All finger gaps (μm)</td>
<td>2</td>
</tr>
<tr>
<td>Lateral springs (l×w) (μm×μm)</td>
<td>250 × 3</td>
</tr>
<tr>
<td>Z torsional springs (l×w) (μm×μm)</td>
<td>300 × 3</td>
</tr>
</tbody>
</table>
LIST OF REFERENCES


[27] Freescale semiconductor, "+-1.5g-6g Three Axis Low-g Micromachined Accelerometer," 2005.


BIOGRAPHICAL SKETCH

Deyou Fang received his B.E. degree in automation control in 1993 from the University of Electronic Science and Technology of China, Chengdu, China. After that, he had been working on design and development of power station control systems for 3 years. From 1996 to 2001, he was with the R&D department at Huawei Technologies Co. Ltd., Shenzhen China, where he had been involved in the design and development of several types of communication equipments, which include telecommunication switches, GSM and CDMA wireless systems, and data communication products. From 2001, he has been a graduate student at the electrical and computer engineering department at the University of Florida, and his research is focused on low-power, high performance interface and signaling circuits design for integrated CMOS-MEMS accelerometers and gyroscopes. He is expected to receive his Ph.D. degree in May, 2006.