ADVANCED THREE-DIMENSIONAL PACKAGING SCHEMES FOR MICROELECTRONIC AND MICROSYSTEM APPLICATIONS

By

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To my family.
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By

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The emergence of GaN-based devices promises a revolution in areas requiring high performance electronics, such as high speed earth and space-based communication systems, advanced radar, integrated sensors, high temperature electronics, and utility power switching. The properties of this system make it ideally suited for operation at elevated temperatures and at voltage and current levels well beyond that accessible by Si. Recent improvements in material quality and device performance are rapidly opening the door to commercialization, and III-N technologies are demonstrating exciting developments of late.

Though devices are entering commercialization, there is still some work to be studied. In particular, GaN high electron mobility transistors (HEMTs) show potential as gas sensors, which will be relevant to the emerging hydrogen fuel cell vehicle market. Devices were fabricated and show a very low detection limit of <10 ppm, and have been integrated in a wireless network that is currently undergoing field testing. Devices have also been fabricated on different substrates such as Si (low-cost), SiC (high performance), and SopSiC (novel material – potentially combines advantages of Si and SiC) to study the effects on device performance and their compatibility with processing for 3-D integration. Reliability testing is a major area of interest. A 32-channel stress test system has been designed and is currently being built.
A 3-D integration project is being undertaken to achieve 3-D bonding of integrated circuits and other components fabricated from dissimilar materials. The thermal design of a vertically integrated multi-chip-module (MCM) based on GaN High Electron Mobility Transistor (HEMT) power amplifiers (PA) on SiC substrates with a backside heat sink/antenna and Si modulator, bonded to a common ground plane using polydimethylsiloxane (PDMS), was studied. Heat transfer was estimated using finite element modeling for different PA power densities, HEMT gate finger pitch, layer thickness, the presence or absence of the thermally insulating layers, and the thickness of dielectric isolation interlayers.

Laser drilling is a promising method for through hole via formation in SiC, presenting several advantages over dry etching, the most important being considerably higher etch rates. Studies have been undertaken to minimize the surface contamination and semiconductor degradation due to this process and, ultimately, make this process competitive with conventional dry etch techniques. By using a UV excimer laser source (193 nm) for drilling, we can achieve considerably better smoothness inside the holes and minimize surface contamination, compared to the use of the more common Nd:YVO₄ laser. The device characteristics of AlGaN/GaN HEMT layers grown on SiC substrates were similar after formation of vias by 193 nm laser drilling to those from an undrilled reference sample. By sharp contrast, 1064, 532, and 355 nm laser drilling produces significant redeposition of ablated material around the via and degrades the electrical properties of the HEMT layers.

Flip-chip bonding is critical for 3-D integration as it is the method that actually forms the bonds. Studies have been performed to look at various materials systems, particularly In, Au, and SU-8 polymer, as candidate materials for flip-chip bonding applications. Bonding protocols have been developed to optimize the mechanical strength of the bond for a MEMS application.
CHAPTER 1
INTRODUCTION

1.1 Motivation

The Gallium Nitride (GaN) materials system is attracting much interest at an industrial level in the late 2000s. Due to the wide-bandgap nature of the material, the material is very thermally stable, and electronic devices can be operated at 500 °C. The material is also chemically stable, with the only known wet etchant being molten NaOH or KOH, making it very suitable for operation in chemically harsh environments or in radiation. This system also demonstrates a high electron mobility, making it suitable for the high frequency communications market, and high breakdown field, making it marketable to the high power industry as well. While this technology has had a very long infancy as researchers strived to develop high quality material on high performance substrates, and develop novel processing schemes to improve device performance to the inherent material limits, it appears in the past couple years that the technology is beginning to mature and move from the lab into production.

1.1.1 Electronic Devices

There is currently strong interest in developing AlGaN/GaN High Electron Mobility Transistors (HEMTs) for use in high power microwave transmission systems, millimeter-wave (MMW) military communications links, and X-band radar systems. Nitride-based HEMTs can operate from very high frequency (VHF) through X-band frequencies with higher breakdown voltage, better thermal conductivity, and wider transmission bandwidths than Si or GaAs devices. GaN-based HEMTs can operate at significantly higher power densities and higher impedance than currently used GaAs devices. The higher sheet carrier density in the two-dimensional electron gas compared to the AlGaAs/GaAs system, and higher electron mobility relative to Si, suggest that nitride-based HEMTs will also exhibit low on-state resistance, an
important advantage for rf applications. Many communications systems for the military operate in the frequency range from 7->44 GHz, and in some cases, the systems are space-borne, where amplifier efficiency, reliability, and low weight are key requirements [1-16].

1.1.2 Three-Dimensional Packaging

As demands on portable devices increase, new packaging techniques must be developed to meet the demands for smaller, lighter, and more functional devices. The early solutions, such as ball grid arrays (BGA) and flip-chip technologies, have met the demands for decreasing package size and interconnect distance and increasing I/O count, but in today’s mobile landscape, the chip footprint area is becoming a huge factor. 3-D packaging solutions meet both the size and performance requirements. Vertical stacking of multiple die within a package, using specialized substrates and interconnects, will reduce the number of chip-to-board connections and decrease the area required for chips and inter-chip wire traces. These techniques are also advantageous from a power consumption standpoint since 40% of power consumption comes from chip-to-chip interconnects. The module-to-board solder connects account for almost 90% of board failures, so reducing the number of connections, we can decrease board failures and attain an overall increase in reliability and decrease in power consumption [17-18].

Laser drilling is a well established method for the machining of metals and hard materials. The mechanism for this process is simple. Essentially, the laser supplies sufficient power to eject the material. The actual ejection mechanism is dependent upon wavelength. At longer wavelengths (532 and 1064 nm), the mechanism is sublimation of the sample and subsequent ejection. As the wavelength decreases, moving into the UV region (355 nm), the mechanism changes to a molecular level bond-breaking phenomenon. This, therefore, results in much cleaner profiles and less redeposited ablation debris. Since the laser can be focused and controlled for much smaller features than standard machining tools, it is an ideal method for
micromachining and scribing. There is current interest in developing laser drilling processes to create through-wafer vias in hard compound semiconductor substrate materials, such as SiC, for both electronic and micro-electro-mechanical systems (MEMS) applications. AlGaN/GaN HEMTs grown on SiC are very promising for high power, high temperature devices due to the superior thermal conductivity of SiC, compared to the original sapphire substrates. Monolithic mm-wave integrated circuits based on these devices will require through wafer via connections to provide a common ground and low inductance path from the source of the FET to the ground plane in the back of the wafer [19-36].

### 1.2 Study Outline

There are four sections of this dissertation. In addition to providing the results of research performed over the past four years, I also wish to share my background knowledge on the subject to create a sort of condensed manuals for future students in the group. To that end, the next couple of chapters will provide purely background information. Chapter two will provide a cursory literature review of compound semiconductors, from initial research and development up to the current state of the art. Chapter three will provide a short summary of device processing, starting with substrate wafer fabrication and the processing steps for device fabrication, all the way up through device packaging, circuit board fabrication, and systems assembly and testing. These two chapters are intended serve as an introduction to the field, and suggest first-day literature for new students to the group.

The next sections will cover research performed over the past four years in detail. This can be divided into two main sections: discrete devices and packaging-level work. Chapters four, five, and six will focus on the devices, and cover efforts to fabricate high performance devices (Ch. 4), gas sensor devices (Ch. 6), and reliability and stress testing (Ch. 5), which is currently a hot topic. Chapters seven, eight, nine, and ten will focus in 3-D packaging work. Topics to be
covered include thermal simulations of a packaged chip to optimize heat transfer (Ch. 7), laser drilling for interconnect formation (Ch. 8), electroless metal plating for thick film deposition (Ch. 9), and flip-chip bonding for assembly (Ch. 10).

The fourth section will conclude my research. This will contain a chapter on future work (Ch. 11), which will outline the steps to be taken to wrap up the current work and suggestions for where to take the work in the future. Chapter 12 will serve as the conclusion, and wrap everything up and tie it together.

The fifth section will be operating procedures. Appendix A will cover operating procedures for processing equipment in the lab, Appendix B will cover electrical testing, and Appendix C will include tables of recipes used in processing. The intent of this section is to consolidate information about the lab. I am a firm believer in leaving somewhere in better shape than it was in when I arrived, and wish to make my contribution by clearly documenting and arranging the necessary information about the lab. I hope that this section can again be distributed to new students on the first day to aid in training, and serve as a master document that is added to and modified by students each year to keep the information current.
CHAPTER 2
COMPOUND SEMICONDUCTOR LITERATURE REVIEW

2.1 Wide Bandgap Electronic Devices

Since the 1970s, III-nitride semiconductors have been considered promising materials for device applications at blue and ultraviolet (UV) wavelengths, much in the same way that GaAs-based and InP-based materials have been commercialized for infrared (IR), red, and yellow wavelengths. AIN, GaN, and InN are all wide bandgap materials and can crystallize in both wurtzite and zinc-blende structures. These materials, along with their alloys, offer an essentially continuous range of direct band gap energies through the visible spectrum and into UV wavelengths. This materials system is, therefore, quite attractive for optoelectronic applications. Applications include light emitting diodes (LEDs), laser diodes (LDs), and detectors. GaN LEDs are essential for development of full-color LED displays, combining, for example, GaN-based blue and green LEDs with GaAs-based red LEDs to form a white LED [37-38].

Another area of interest for III-N materials is the high temperature and high power electronics market. These materials are perfectly suited for such applications due to their wide bandgap nature and high breakdown fields. Due to the wide bandgap, these materials become intrinsic at much higher temperatures than Ge, Si, or GaAs, allowing for fewer high-cost processing steps and design issues to maximize cooling. The breakdown field scales with the square of the band gap, so, again, the wide bandgap materials demonstrate higher breakdown fields, allowing for potential use as a replacement for vacuum tubes in the utility industry. GaN in particular shows excellent transport properties, including high carrier mobility and high drift velocity, making it suitable for general electronics, particularly microwave devices. This allows for the exploitation of three regimes which have previously been unattainable: high temperature, high power, and high frequency. Perhaps the best feature of III-N materials is the heterostructure
technology. These materials can support quantum well, modulation-doped heterointerface, and heterojunction structures. Also attractive is the exceptionally high thermal and mechanical stability [37, 39-42].

Research on III-N growth began in the 1960s. One difficulty encountered is the lack of available substrates. For this reason, efforts were essentially stopped on III-N growth during the 1970s and 1980s. Given the constraints, sapphire (Al2O3) and SiC are the most popular substrates currently used. Bulk GaN wafers would be ideal, but that technology has yet to be developed. SiC is a particularly interesting substrate due to its high thermal conductivity (~350 W/m-K). Metal organic chemical vapor deposition (MOCVD) has emerged as the choice method for growing GaN due to its high degree of compositional control and uniformity, availability of high purity sources, and large scale manufacturing compatibility [37,43].

One key parameter for a GaN film is defect density. There has been considerable progress in the last decade on epitaxial growth techniques and heterostructures, which will minimize defect density and allow for device fabrication. Another issue with wide bandgap growth is the doping. Native defects, particularly nitrogen vacancies, make the MOCVD material predominantly n-type; however, progress has recently been made allowing MOCVD growth of p-type material [37, 44-46].

The first p-n junction LED was demonstrated in 1989 by Amano et al. Nichia Chemical Industries was the first to commercially produce blue LEDs following this breakthrough with very high efficiency and intensity. Nakamura et al first reported current-injection GaN LDs in 1996 and subsequently achieved continuous wave (CW) lasing at room temperature. It is interesting to note that these devices were achieved while still in the stage of low quality film
growth. The dislocations did not appear to be efficient non-radiative centers, so while optical devices could be achieved, the defects do affect reliability [37, 47-50].

Rapid progress has been demonstrated in field effect transistor (FET) structures. This places very strict demands on the growth and processing, but the technology has been developed in the past decade, and present published results indicate that GaN will play a significant role in the development of high temperature, high power, and high frequency electronic devices. Further improvements in materials quality will enhance device operation, though processing technology must also be improved for significant development. There are many processing issues, such as poor p-type doping, low resistance and thermally stable ohmic contact development, high temperature requirements for implant activation, poor wet etching processes, low dry etch rates, and other issues. As advances are made, we can expect further improvements in device performance and increasing commercialization [37, 43].

2.2 High Electron Mobility Transistors

High Electron Mobility Transistors (HEMTs) have emerged in the past twenty years as promising candidates for microwave and high voltage applications. HEMTS were originally based on AlGaAs/GaAs, AlGaAs/InGaAs, AlInAs/InGaAs, and related systems on GaAs or InP substrates. In the 1990s, AlGaN/GaN HEMTs on sapphire, SiC, or even bulk GaN substrates have demonstrated considerably larger power density (>12 W/mm), and have become contenders for high power amplification and switching applications. The use of wide bandgap semiconductors presents an advantage because, in addition to the increased output power, the temperature tolerance and radiation hardness is also extended. Recently, GaN-based HEMTs have been demonstrated operating at 750 °C [43].
The HEMT is also known as MODFET (modulation-doped FET), TEGFET (two-dimensional electron gas FET), SDHT (Selectively Doped Heterostructure Transistor), or HFET (Heterojunction FET). The defining feature of a HEMT is the channel formed by carriers accumulating along an asymmetric heterojunction. A schematic of a GaN/AlGaN heterostructure is shown in Figure 2-1. There is a large conduction band discontinuity, causing the electrons to diffuse from the AlGaN (large bandgap) into the GaN (small bandgap), forming a two-dimensional electron gas (2DEG) in the triangular quantum well at the interface. The carrier density is further enhanced in GaN by a strong piezoelectric effect [37, 43, 51].

The conceptual physics of the HEMT were first discussed as early as 1969 [54]. The development in the 1970s of MOCVD and MBE techniques allowed for the growth of heterojunctions. Mobility enhancement in an AlGaAs/GaAs heterojunction was demonstrated in 1979, which led to the demonstration of the first HEMT in 1980 [55-57]. Although GaN growth was first studied in the 1960s, suitable substrates and growth technology did not catch up until the late 1980s. Mobility enhancement in AlGaN/GaN heterojunctions was first demonstrated in 1991, with HEMTs for microwave applications being demonstrated in 1993 [58-59]. Considerable progress was made during the 1990s in the areas of material quality, heterostructure design, and ohmic contact formation, and the first high power devices were demonstrated in 1997 [60-61]. Khan demonstrated the first AlGaN/GaN HEMT in 1993, reporting a $g_m$ of 23 mS/mm, $f_T$ of 11 GHz and $f_{\text{max}}$ of 14 GHz [37, 43, 51-53].

To demonstrate the progress in the field since the early developments, some recent statistics will be reported. Due to high 2DEG sheet carrier concentration and saturation velocity, power density of nitride HEMT has been reported over 30 W/mm [67]. A research group from Japan has recently reported a power output of 370 W at 2 GHz. This demonstrates the superiority
of GaN over GaAs and Si, which are very mature technologies, and have maximum power outputs reported in the range of 200-300 W and power density of 2W/mm [62]. This is ideal for W-CDMA base station applications. This type of performance is typically achieved with a large periphery device (in this case 120 fingers of 400 μm each), which can be realized in a controlled mass production environment. (power matching issue will reduce the efficiency) This particular device employed a high performance SiC substrate that was thinned and had thermal vias for improved heat transfer. This type of structure cannot be realized in a cost-effective manner for mass production. Commercially available devices are available though. Nitronex corporation, for example, offers devices operating up to 4 GHz with output powers up to 180 W at a production environment that can be scaled up to a high throughput level by using GaN on Si. The particular advantages of substrate choice will be discussed in Chapter 4 [63].

A high breakdown voltage is required for proposed For high power switching applications, devices with high breakdown voltage are preferred, which can be operated at lower current level to reduce the diameter of the cable. A research group at Cornell has recently reported HEMTs with an off-state forward breakdown (gate completely pinched off) of 1350 V for a gate-drain distance of 16 μm. This employed a high resistivity carbon-doped GaN layer for high breakdown and low leakage. The calculated breakdown field is about 1.6 MV/cm, which is approaching the theoretical limit for this material [64]. Simple calculations can then prove that devices with breakdown voltages in the tens of kV range can be fabricated easily by pushing the gate to drain distance larger. Some work in this area will be discussed in Chapter 4.

The third realm that GaN is important for is the high frequency market. Maturation of processing techniques and of device structure has been used to eliminate the parasitic effects seen in early HEMTs that limited RF performance. On the processing side, a group in Japan has
increased 2DEG carrier density by depositing a catalytic CVD process for nitride passivation, a high aluminum content barrier layer, and a short gate length. This group was able to achieve a 30 nm gate contact length using a T-gate architecture. The reported unity gain cut-off frequency, $f_T$, of over 180 GHz is almost double any previously reported value, due primarily to the short gate length [65]. Other groups, in particular Palacios at UCSB, have reported structure optimization to improve small-signal gain [66]. This work focused in obtaining a high $f_{\text{max}}$ by minimizing parasitic resistances and capacitances in the device structure based on the small signal equivalent circuit (discussed in Appendix B). An InGaN layer was inserted below the AlGaN layer, with a thin InGaN layer between AlGaN and GaN. This serves to create a double heterojunction. The conduction band is raised at the InGaN/GaN interface on the GaN side relative to the InGaN channel. This improves confinement and reduces short-channel effects, creating a higher output resistance. Parasitic capacitances were reduced using field plate technology (discussed below), resulting in a reported $f_T$ of near 130 GHz and a record $f_{\text{max}}$ of 230 GHz [66].

The HEMT is a lateral current flow device with ohmic source and drain contacts and a Schottky gate contact. A schematic is shown in Figure 2-2. Device isolation is typically achieved by either etching through the AlGaN layer and partially into the GaN layer with a Cl$_2$-based plasma to confine the 2DEG, or by implanting the material with a heavy dose of He$^+$ or N$^+$ ions to create a thick layer with high resistivity. Ohmic metallization is accomplished using lift-off a metal stack that is typically Ti-Al based. Such formulations include Ti/Al/Pt/Au and Ti/Al/Ni/Au, with rapid thermal annealing used to alloy the metal at temperatures from 850-950 °C for 30-60s. Specific contact resistances are typically around $1 \times 10^{-6} \ \Omega \cdot \text{cm}^2$. Gate contacts are a stack of either Ti, Ni, or Pt and Au. The gate can be patterned by optical lithography down to 1 μm dimension and e-beam lithography can be used to pattern gate length down to 100 nm. A
final metal layer is used to route out the device contacts to bond pads for probing and bonding to a carrier. This is typically a stack of either Ti/Au or Ti/Pt/Au and is usually relatively thick, around 3000 Å.
Figure 2-1. Energy band structure of AlGaN/GaN heterojunction

Figure 2-2. Cross-section of an AlGaN/GaN HEMT
CHAPTER 3
SEMICONDUCTOR PROCESSING

3.1 Overview

This chapter is meant to give an overview of semiconductor material growth and device processing, starting from raw materials all the way up to a functioning circuit board.

3.2 Crystal Growth

The first step towards microelectronic devices fabrication is the substrate wafer growth. In a melt process, the raw materials (ultra high purity Si, for example) are simply melted and resolidified in single crystal form. The process is much more complicated than this, as a considerable amount of control is required to maintain crystal orientation and impurity concentration over the large quantities of material grown. A related technology is the growth of thin single crystal layers on the single crystal substrates. This process is called epitaxy. This process is particularly important for high-performance devices because it allows for precise control of layer thickness and impurity doping concentration. At the current technology level, high quality Si and GaAs wafers grown from the melt are widely available, while GaN is grown epitaxially (bulk GaN wafers are available, but they are still grown epitaxially and are of poor quality) [69].

3.2.1 Growth from Melt

Silicon is typically grown using the Czochralski method (CZ growth). The starting material is quartzite, which is a pure form of sand (SiO₂). It is refined to form ultra high purity polycrystalline silicon (99.999999999% pure) through various treatments. The first is reduction in a furnace using carbon, shown in reaction 3.1. This is followed by a HCl treatment to dissolve the Si, shown in reaction 3.2. The solution is distilled to remove impurities, followed by a
hydrogen reduction to recover the solid electronic grade silicon. This reaction is essentially the reverse of reaction 3.2. The reactions are given below: [69]

\[
\begin{align*}
\text{SiC (s) + SiO}_2 \text{ (s) } &\rightarrow \text{ Si (s) + SiO (g) + CO (g)} \quad (3.1) \\
\text{Si (s) + 3HCl (g) } &\rightarrow \text{ SiHCl}_3 \text{ (g) + H}_2 \text{ (g)} \quad (3.2)
\end{align*}
\]

This high quality poly-Si is then melted in a silica crucible in a vacuum chamber (melting point = 1412 °C). A small seed crystal is lowered into the melt and slowly withdrawn. Freezing will occur at the interface, yielding a large single crystal. These are referred to as boules or ingots. Modern silicon ingots can be 400 mm (16 in) diameter and 2 m long. The pull rates are very slow, on the order of mm/min, to balance the heat transfer. A schematic of a crystal pull system is shown in Figure 3-1 [68].

Control of impurity concentration is critical. Magnetic fields are typically added to crystal pullers to prevent the incorporation of ionized impurities. A float-zone process can also be used to refine the ingots and further remove impurities. In this process, RF heating is used to melt a small cross section of a polycrystalline or single crystal rod. As this coil traverses the length of the rod, impurities will follow the molten region, ultimately being concentrated at one end of the rod. A schematic of a float zone system is shown in Figure 3-2. This growth method is limited in that the melted region must be able to support the weight of the entire crystal, so ingots of only a few kilograms can be refined [68].

The major difficulty in producing large compound semiconductor ingots from a melt is maintaining the stoichiometry from the melt to the solid. In all methods, an overpressure of the more volatile component is required to prevent preferential loss. In the case of GaAs, the stiochiometric solid is synthesized first by placing high purity solid Ga and high purity As in a sealed two-temperature furnace, heating each component to the melting point. The melting point
of As is lower (610 °C), so an overpressure of As will form, causing transport of As to the Ga melt (1240 °C), forming GaAs, then cooling the melt. From the raw material, ingots can be formed by the Czochralski method and the Bridgman method. The Bridgman process is very similar to the material synthesis process. An overpressure of As is created in a lateral furnace to prevent decomposition, and the polycrystalline GaAs is placed with a seed in a high temperature zone of the furnace. The furnace is moved so that the material will melt and then freeze following the seed. This process can be compared to a horizontal float-zone process. A schematic is shown in Figure 3-3 [69].

After growth, wafers are prepared from the ingots for fabrication. The seed and tail ends are cut off, the ingot is ground to a uniform diameter, and flats are ground along the length of the crystal to define crystal orientation and conductivity type. Standard flat orientations are shown in Figure 3-4. A diamond saw is used to slice the crystal into wafers (thickness of 500-700 μm), which are then lapped to a flatness of around 2 μm, etched to remove contamination, and polished on one or both sides for device fabrication [68].

3.2.2 Epitaxial Growth

Epitaxial growth methods are used to grow single-crystal semiconductor layers on single-crystal substrates. Homoepitaxy is the term used to denote growth when the substrate and the grown layer are the same, for example growth of a highly doped layer of GaAs on a single crystal bulk GaAs substrate. Heteroepitaxy is used to denote growth of a semiconductor layer on a different substrate, such as GaN on SiC, or AlGaAs on GaAs. The growth systems used must be highly precise. The layers must be of nearly perfect quality and have atomically smooth interfaces. The most common growth methods are chemical vapor deposition (CVD), metal organic CVD (MOCVD), and molecular beam epitaxy (MBE). Since epitaxial growth involves a
chemical reaction, where the melt processes were mainly physical, kinetics are very important. The kinetics of MOCVD growth are a subject or continued research at present, and a better kinetic understanding of reaction phenomena will ultimately lead to better material quality and higher performance [69].

MBE uses pure atomic sources, directed as thermal beams, which react at the surface. The advantage of this method is that precise control over composition and doping can be achieved, however growth rates are typically slow, less than 1 μm/h. Though slow, this system presents the ultimate performance in terms of control, cleanliness, and characterization capabilities. MBE systems operate under ultrahigh-vacuum (10⁻⁸ Pa), so there is minimal contamination, and characterization equipment can be integrated for in-situ SEM or XPS analysis of the films. High temperature baking steps are used to prepare the surface for MBE by removing native oxide or other adsorbed species. It is a relatively low temperature process (400-900 °C), and combined with the low growth rate, many unique structures can be created, such as the superlattice structure (periodic structure consisting of layers <10 nm thick). A schematic of an MBE reactor is shown in Figure 3-5 [69].

MOCVD has emerged as the choice method for growing GaN, and III-V compounds, due to its high degree of compositional control and uniformity, availability of high purity sources, and large scale manufacturing compatibility. This method is particularly advantageous for those materials that do not form stable hydrides or halides. Another advantage is that the organic precursor compounds are volatile at low temperatures, and liquid Ga is not required. In general, the precursors are the trimethyl-III (ex, trimethylgallium (TMGa), trimethylaluminum (TMAI)) and V-H3 (ex, arsine, AsH3, ammonia, NH3). The material is typically doped with zinc, cadmium, or silicon, so diethylzinc, diethylcadmium, and silane are used as the sources. Safety is
a particular concern when dealing with these systems due to the dangers associated with these precursors (silane is highly flammable, arsine is toxic, etc). There are three main components of an MOCVD system: gas delivery, reactor, and exhaust. Typically the organometallic sources are enclosed in bubblers, with hydrogen as the carrier gas, and the group V source as a compressed gas. Extreme care must be taken in the delivery system to avoid condensation or pyrolysis of the organometallic precursors. A general issue is the gas flow pattern and introduction into the chamber. To obtain atomically smooth interfaces, the valves must be designed so that there will be no perturbations as flows start and stop. A schematic of an MOCVD reactor is shown in Figure 3-6 [68].

3.3 Dopant

Impurity dopant is used to change the electrical properties of semiconductors. It is an important step in every device fabrication process since it creates the p-n junctions that are the key active parts of the devices. The doping process must be very tightly controlled and reproducible. It is critical to control the process both in terms of introducing the impurity concentration to design specifications and controlling the area where the impurity is introduced. There are two methods of doping semiconductors: thermal diffusion, which is typically used to create deep wells, and ion implantation, which is used to create precise shallow junctions or very high impurity concentrations [69].

3.3.1 Diffusion

Diffusion is a fundamental transport phenomenon that involves the redistribution of free material in response to a concentration gradient. The material flux is proportional to the concentration, and movement will be away from the high concentration region towards the region of lowest concentration. There are two basic atomic diffusion mechanisms in semiconductor crystals: movement through vacancy lattice sites, and movement through
interstitial sites. The basic governing equation is known as Fick’s first law of diffusion, shown in equation 3.1 below, with the diffusion coefficient, $D$, in $\text{cm}^2/\text{s}$. The diffusion coefficient is temperature dependent and follows an Arrhenius law [69].

\[
\frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2} \tag{3.1}
\]

The differential equation can be solved analytically for two important cases: constant source and constant impurity material. In the former case, the boundary conditions are: $C(x,t=0) = 0$, $C(t,x=0) = C_s$, $C(x=\text{inf}, t = 0)$. The solution is shown below in equation 3.2, where erfc is the complimentary error function. In this case, the surface concentration is determined by the solubility of the dopant in the crystal and the depth profile is determined by time. [69]

\[
C(x,t) = C_s \text{erfc} \left( \frac{x}{2\sqrt{Dt}} \right) \tag{3.2}
\]

For the latter case, the boundary conditions are: $C(x=\text{inf}, t = 0)$, and $Q = \text{const}$ (total dopant quantity). The solution is a Gaussian function of the form shown in Equation 3.3. In this case, the material will move into the semiconductor, but the surface concentration will decrease. [69]

\[
C(x,t) = \frac{Q}{\sqrt{\piDt}} e^{\frac{x^2}{4Dt}} \tag{3.3}
\]

In most semiconductor thermal diffusion processes, both of these conditions are used. First, what is called a *predeposition* step is used to introduce the required quantity of material. This is considered a constant source diffusion process. The source can be either a solid, liquid, or gas. After this step, a second step called a *drive-in* is used to quite literally drive the dopants into the material and redistribute to the desired concentration profile. [69]

Thermal diffusion gives very good reproducibility, and concentration profiles can easily be calculated using simulation software such as SUPREM. The problem with thermal diffusion is
that any later diffusion or thermal oxidation steps will cause redistribution of the dopants that are already in the material, so the combined effect of multiple temperature cycles must be considered. It is therefore undesirable for shallow junctions as they cannot be controlled as well. It is still used to form deep junctions and as an alternative to ion implantation when crystal damage is an issue. For compound semiconductors, ion implantation almost exclusively used. As mentioned in previous sections, high temperature processes for long time periods can cause preferential loss of one component, so these materials are more compatible with low temperature processing unless capping layers are used [69].

3.3.2 Ion Implantation

Ion implantation uses charged particles to introduce impurities into the material. The ion dose can be controlled by monitoring the ion current, making it very attractive for shallow or lightly doped junctions. The principle of operation is as follows: a heated filament breaks up source gas into charged ions, which are extracted from the source. The specific ion to be implanted is selected using a mass analyzer to filter by mass to charge ratio. The ions are then accelerated toward the sample at 10-400 kV, where they strike the samples and penetrate to a given depth, with a distribution determined by the ion dose, accelerating voltage, and type of ion. A schematic of an ion implantor is shown in Figure 3-7 [68].

There are two stopping mechanisms: electronic stopping, where the attractive power of electrons in the lattice eventually slows the ion and stops it, and nuclear stopping, where collisions with nuclei in the lattice cause energy loss and ultimately stopping of the ion. It is possible for ions to travel down channels created by the crystal planes, so most commercial systems tilt the sample at 7-10 degrees relative to the major plane. As the ion travels into the lattice, it will displace nuclei, causing lattice damage and in the case of high doses, amorphization. When ion implantation is used, a post-implant anneal step is required to
recrystallize the material and remove damage. In some cases, a sacrificial layer of oxide or nitride can be used to protect the surface from significant damage and alter the profile. The implanted profile typically follows a Gaussian distribution and can be calculated using SRIM software code [69].

3.4 Film Deposition

Film formation and patterning constitutes a basic device building block. There are actually four general types of thin films: thermal oxide, dielectrics, polysilicon, and metal. Since this work focuses primarily on compound semiconductors, thermal oxidation and polysilicon deposition will not be discussed in detail, but will be briefly mentioned here.

Thermal oxidation of silicon is well documented, and is used to form both thin and thick native oxide layers. Typical growth conditions are either flowing dry oxygen – slow growth rate, high quality - or flowing “wet” oxygen (oxygen bubbled through water) – fast growth rate but lower quality – at temperatures of 900-1200 °C. The growth rate is dependent upon thickness, since for thicker films the oxygen must diffuse through the film to reach the silicon surface to react, and equations are available to determine growth time to reach a given thickness [69].

Polycrystalline silicon is primarily used for the gate electrode in silicon MOSFETs because it has better reliability than aluminum. It is deposited in a CVD reactor by the pyrolysis of silane at 600 °C to form silicon and hydrogen. The parameters that affect this process are primarily deposition temperature and the addition of any dopant gas [69].

3.4.1 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is typically used to deposit dielectric films. There are three variations of the CVD process: atmospheric pressure CVD, low pressure CVD, and plasma enhanced CVD (PECVD). The considerations in selecting the process include temperature, rate,
quality, morphology, and electrical properties. Atmospheric CVD is particularly advantageous in that it allows for a continuous feed system since no pumping is required, and it has high deposition rates. The reactant gas is simply injected to a showerhead above the wafers on a heated chain track. The disadvantage to this system is the poor quality and the particle contamination associated with atmospheric pressure processes. Low pressure CVD is very popular in the IC business because, while a batch system, it allows for high throughput and excellent uniformity. PECVD offers the advantage of low temperature processing and the ability to integrate with a cluster tool, but uniformity can be poor [68].

Silicon nitride and silicon oxide are the dielectrics primarily used with compound semiconductors. Silicon nitride in particular is important as a passivation and capping material. It oxidizes very slowly, serves as a diffusion barrier to water and sodium, and has a slower etch rate in buffered HF than silicon dioxide. Silicon dioxide can be deposited by thermal oxidation on Si, or on any semiconductor by LPCVD or PECVD using silane, NO, and nitrogen. Atmospheric CVD can be used to deposit silicon films containing 4-12% phosphorous or boron (phosphosilicate or borosilicate glass – PSG or BSG). Silicon nitride is very difficult to grow thermally, so LPCVD or PECVD are typically used to react silane and ammonia. It deposits as an amorphous dielectric, and can contain hydrogen. This is especially true in PECVD, where the nitride is rarely stoichiometric (Si$_3$N$_4$), and instead is denoted as SiN$_x$, with up to 25% hydrogen. The quality of the film can be determined immediately by comparing the refractive index measured by ellipsometry to that of an ideal stoichiometric film [69].

3.4.2 Metal Deposition

While metal can be deposited using CVD from metalorganic sources, most metal films are formed by physical vapor deposition (PVD). Two common methods are evaporation and sputtering. The mechanism is simple – the metal atoms are ejected from the source into a
vacuum, where they land on the sample of interest. In the evaporation method, a metal crucible is heated either resistively, inductively, or with an electron beam, and emits metal vapor. The vapor travels through the vacuum and lands on all surfaces in the chamber. Evaporation typically gives poor step coverage because the atoms are very directional as they approach the surface. This can actually be advantageous in a lift-off process (described below). The deposition rate is monitored by a crystal monitor, which is a thin film oscillator. As particles accumulate, the resonant frequency of the oscillator changes in a very predictable manner, and therefore can measure film thickness with angstrom level precision. The deposition rate will be proportional to the vapor pressure of the metal at the charge surface and the distance from the charge to the sample. A problem with evaporation is that it is difficult to deposit alloys. Alloyed charges cannot be used unless the vapor pressure of both metals is similar at deposition temperature, otherwise there will be preferential deposition of the more volatile component. A rotating shutter can be used to alternate deposition, but this can be costly since multiple charges and heaters are required. Evaporation is used extensively in the compound semiconductor industry because of the capabilities to deposit a wide range of metals, and the capabilities to load multiple charges and form stacks of different metals [68].

Sputtering involved the physical bombardment of a target metal sample by ions (typically argon), resulting in the ejection of material into the chamber, which deposits on the surface of the sample. Because the process involves charged particles, there is the possibility of damage to the semiconductor surface, but heating of both the sample and the metal and chamber is less of a concern. It is particularly easy to sputter alloys, and sputtered atoms are less directional, so step coverage is improved. Since the sputtering process is physical bombardment, it will not be
selective, so sputtering of an alloy should result in a similar composition in the film and the original target. For these reasons, sputtering is used extensively in the silicon IC industry [68].

There are two methods of patterning metal films – additive and subtractive. In the subtractive process, the film is deposited first, then patterned and etched. This is widely used for aluminum patterning, since a selective etchant is readily available (PAN etch = phosphoric, acetic, nitric acid solution). The additive method, or lift-off method, is used for patterning metal stacks used in compound semiconductor devices. In this process, the pattern is formed in photoresist, then the metal is deposited over this film, then the film is removed, leaving behind the metal on the substrate. The yield is usually lower for this process, particularly for small features [69].

3.5 Lithography

Lithography is the most complicated, critical, and expensive process in semiconductor fabrication. It is the process for forming patterns on the semiconductor substrates for film deposition, film removal, or doping. It is the primary driving force for growth in the industry, as it defines the minimum feature size. Improvements in lithographic techniques to make smaller features will improve chip performance more than any other technology described in this chapter. This step is repeated for almost every layer in the device structure, and therefore represents about 35% of IC manufacturing cost. For these reasons, it is the most significant economic factor in IC manufacturing [68].

3.5.1 Photoresists

Photoresists are polymers that are sensitive to radiation at a given wavelength. When selectively irradiated through a mask, a chemical change will occur that makes them either more soluble or less soluble in what is known as a developer solution than the surrounding matrix that has not been irradiated. In this manner, a pattern can be transferred from the mask to the
semiconductor surface. This will selectively open or protect areas for doping, etching, and film deposition. There are two basic types of resists: positive tone and negative tone. In the positive resist case, the area that is exposed through the mask is removed, therefore duplicating the mask pattern on the surface. In the negative resist case, the area that is not exposed is removed, leaving the area that was exposed. This creates the reverse image from the original mask. A pattern formed by positive and negative resists is shown in Figure 3-8. Both have applications in industry, some examples being as follows: positive resists are used to open areas for doping, dielectric window etching, and metal lift-off, and negative resists used to mask transmission lines in a metal film while the rest is etched off. Positive resists tend to offer better resolution and fewer environmental hazards, and therefore are used almost exclusively in industry [68].

Photoresists are applied by spin coating. The film thickness is a function of both the spin speed and the viscosity. After spin coating, the resists are baked on either a hot plate or an oven to remove the solvent. Resists are identified by a 4-digit number. The first two digits are the series, and the last two digits identify the thickness. For example, Shipley S-1808 is a 1800 series resist that is 0.8 μm thick at 5000 RPM, and S-1818 is a 1800 series resist that is 1.8 μm thick at 5000 RPM, while S-1045 is a 1000 series resist, and is 4.5 μm thick at 5000 RPM.

Optical resists typically consist of three components: a polymer resin, a photoactive compound (PAC), and a solvent to control the mechanical properties. The typical positive resist uses novolac (N) as the resin and xylene and acetates as the solvent. The solvent is primarily used to adjust the viscosity for coating, then baked off before exposure. The most commonly used PAC is diazoquinone (DQ). Before exposure, the molecule acts as an inhibitor, slowing the dissolution rate of the N resin, which is normally very soluble in aqueous solutions. Exposure to UV light causes the loss of N₂ from the carbon ring. The active site is stabilized by a Wolff
rearrangement. In the presence of water, the structure rearranges once more to form a carboxylic acid. The DQ molecule and the subsequent reactions are shown in Figure 3-9. The carboxylic acid will readily dissolve in a base solution. The typical positive resist developing solutions are KOH-based (example: Clariant AZ-400K) or tetramethylammonium hydroxide (TMAH: (CH₃)₄NH₄OH)-based (example: Microchem MF-321) solutions diluted with water and surfactants added. The positive resists have better resolution because the unexposed areas are unaffected by the developer and the novolac resin is very resistant to chemical attack. A disadvantage is that for some semiconductors, such as Si, there can be adhesion trouble. To get around this problem, the wafers are primed with hexamethyldisilazane (HMDS), which is an adhesion promoter [68].

Negative resists work by cross-linking under UV exposure, making the exposed areas less soluble. As such, there is a wider variety of negative resist resins, but one class is azide-sensitized rubbers such as cyclized polyisoprene. A post exposure bake is usually required to complete the cross-linking reaction, and the developer is typically an organic solvent. The advantage of negative resists is the short exposure times required to promote cross-linking, and good adhesion to substrates. The disadvantage is that the resist swells during development, which can cause broadening and distortion of lines. Therefore negative resists are not suitable for high resolution applications [69].

For metal lift-off processes, an overhanging structure is desired to create a discontinuous film that can be removed. There are several options available for this. The one primarily used involves soaking the resist in either toluene or chlorobenzene. These molecules will be absorbed by the top layer of resist and bond with some of the PAG sites, decreasing the sensitivity of the resist to light. The bottom part of the resist is unaffected. After exposure, the
top layer will develop more slowly, creating an overhang. Other new technology involves the development of special lift-off resists (LOR), which are used in a dual layer system. LOR is not photoactive, and is more soluble in the developer than the regular photoresist. During development, after the developer goes through the positive resist layer, it will dissolve the LOR isotropically, creating the overhanging structure [68].

A third class of resists that must be discussed are electron-beam resists. Nonoptical resists are typically long chain polymers. Irradiation of these polymer chains by either electron beam or X-ray radiation will cause either chain scission or cross-linking, creating positive and negative tone images, respectively. Most nonoptical lithography is positive tone, and the most commonly used resist is polymethyl methacrylate (PMMA). Chain scission and cross-linking occur, but the rate of chain scission is much higher, therefore it creates a positive image. During development, the longer chains will be more soluble in the developer, and the chains that have been cut will develop faster. The developer therefore is just an organic solvent, typically a solution of methylisobutyl ketone (MIBK) and isopropanol (IPA). Like optical resists, the PMMA is dissolved in an organic solvent, such as anisole, for storage and coating. The solvent is baked off before exposure. PMMA itself has only fair sensitivity to the electron beam. For a lift-off process, a layer of a more sensitive polymer, such as a PMMA-MAA copolymer (MAA = methyl acryl acrylate) can be applied first and baked, then coated with PMMA alone. This will create an overhanging structure that is suitable for lift-off, shown in Figure 3-10 [68].

3.5.2 Optical Lithography

Optical lithography is the true workhorse of the industry for pattern generation. A typical CMOS process can involve 15-20 lithography steps, almost all of which are achieved by optical lithography. In this method, the photoresist is patterned using optical radiation, typically in the UV range using a mercury arc lamp. Some standard wavelengths are the g-line (465 nm) and I-
line (365 nm). Resolution is limited by diffraction to about the wavelength of light used. Efforts are underway to reduce the wavelength by using xenon as a fill gas in the lamp or using excimer lasers. A simple optical lithography system is shown in Figure 3-11 [68].

The basic feature characteristic to optical lithography is exposure through a photomask. The mask is a quartz plate with a chrome metal layer on one side that is patterned. The mask is designed using computer software such as SPICE or L-Edit, then transferred to the mask using a high resolution lithography system such as e-beam lithography, or patterned using optical lithography using a transparency page from a high resolution laser printer as the mask. The master mask can then be used to transfer the pattern to the semiconductor substrates using photoresists as described above [68].

The basic components of an optical lithography system will now be described. As mentioned previously, the light source is a high-pressure mercury arc lamp. There is a series of reflectors inside the lamp housing to collect light and direct it towards the wafer. There is then a series of apertures and homogenizers to ensure the beam is uniform over the wafer area, and collimate and shape the radiation. Finally, there is a filter to select the appropriate wavelength from the emission spectrum, and then there is a shutter to control the exposure of the wafer [68].

There are multiple exposure methods, which will ultimately affect the resolution of the pattern and the lifetime of the mask. The method used in research is referred to as hard contact. This means that the mask is pressed against the substrate. This close contact will achieve the highest resolution, but there will be considerable wear and damage to the mask master. This is required to achieve submicron resolution. A second method, referred to as proximity exposure, leaves a gap of anywhere from a few to tens of microns between the mask and the wafer. While this significantly reduces wear on the mask, it has poor resolution. Projection printers are used
almost exclusively in industry. These systems use a series of lenses to demagnify the mask pattern and focus it on the wafer. This method can achieve the high resolution of contact lithography with minimal mask wear. The first systems were simply 1:1 projectors. These systems have since been replaced with step and repeat systems. Rather than simply project the mask pattern onto the sample, a reticle containing just one cell or chip is imaged. A 10:1 or 5:1 reduction lens is used to demagnify the mask on to the wafer, and then mechanically stepped to the next cell. Since there is a demagnification factor associated with this process, ultra high resolution can be achieved. A state of the art stepper system can pattern <0.5 um features over a 2.5 cm chip and accurately step the chips over a 40 cm wafer. A particular advantage of these systems is that they automatically adjust alignment and focus at each site, so wafer bowing can be compensated [68].

3.5.3 Electron Beam Lithography

To further reduce feature size, efforts have been made to use short wavelength, non-optical sources, such as X-rays and electron beams. Electron beam lithography (EBL) systems are direct-write systems. These systems are essentially a SEM system with a built in pattern generator and stage translation components. They consist of an electron source (typically a W filament), extractor cage to accelerate the electrons toward the wafer, and series of apertures and condenser lenses to focus the beam. Deflection coils are places immediately before the pole piece to direct the beam over a given area. The exposure is performed by a combination of beam deflection and stage translation, similar to a stepper system. The stage steps to one cell, called a stitch field, and the beam is deflected over that area to form the pattern. The stage then moves to the next field, and the beam is deflected, and so on. The stitch field is a square from 100-1000 μm per side. Another consideration in the exposure process is the proximity effect. Electrons
penetrate the wafer and are scattered, and can re-emerge from the wafer. This is in fact one method of detection in an SEM. These backscattered electrons will affect the irradiation in neighboring areas of the pattern. It is possible to simulate these effects and correct the dose on regions that are close enough to experience this effect. A schematic of the electron beam system is shown in Figure 3-12 [68].

The major disadvantage of the EBL systems is that the throughput is extremely low since it is a serial direct-write process. Exposure of just one wafer can take an hour or more because the stage has to step and expose every stitch field. For this reason, they are excellent for research level fabrication where small features are required (minimum feature size can be <50 um), but impractical for mass production. This represents one of the fundamental challenges for the industry over the next 10 years – how to push the limits of optical lithography to this resolution to maintain the throughput [68].

3.6 Etching

Etching is used to remove material through a mask patterned by lithography. There are two basic types of etched: wet and dry, both with their own advantages that will be discussed. The differences between wet and dry etching in terms of pattern transfer are shown in Figure 3-13 [69].

3.6.1 Wet Etching

Wet etching is a purely chemical attack of the material. It is primarily used to etch dielectrics such as SiO₂ and SiNₓ. There are three basic steps in the reaction mechanism – diffusion of etchant to the surface, chemical reaction, and diffusion away from the surface. That being said, there are two types of wet etch – diffusion limited and reaction limited. The majority of wet etched are diffusion limited, so an acid spray can be used to continuously supply fresh etchant to the surface to enhance the etch rate and the uniformity. Since both the reaction and
diffusion are temperature dependent, precise control of the bath is required for reproducible etch rates [69].

Wet etching of SiO$_2$ and Si$_3$N$_4$ is performed in a buffered hydrofluoric acid solution, known as buffered oxide etch (BOE). Typical ratios are 6:1, 10:1, and 20:1 water to HF. The solution is buffered with NH$_4$F to maintain a fresh supply of HF. The solution is selective to silicon dioxide over silicon 100:1, and etch rates are around 1000 Å/min. The reactions are shown below.

$$\text{SiO}_2 + 6\text{HF} \rightarrow \text{H}_2 + \text{SiF}_6 + \text{H}_2\text{O}$$

$$\text{NH}_4\text{F} \leftrightarrow \text{NH}_3 + \text{HF}$$

Silicon nitride can also be etched in BOE, at a rate of about 1/3 that of oxide, depending on the quality of the nitride. PECVD nitride can be etched at nearly the same rate asoxide if there is a significant amount of hydrogen incorporation. Silicon alone can be etched by a solution of HNO$_3$ and HF, and selectively etched along the (100) plane over the (111) plane by KOH. Doping-selective etches are also available, and a solution of HF/HNO$_3$/CH$_3$COOH will selectively etch heavily doped layers of Si. Defects etch preferentially, so wet etching can be used to stain defects and make them visible in even an optical microscope to calculate defect density. Wet etches for GaAs are based on mixtures of peroxide and acid, such as H$_2$SO$_4$/H$_2$O$_2$/H$_2$O. Similar mixtures using NH$_4$OH or H$_3$PO$_4$ instead of H$_2$SO$_4$ can be used to selectively etch AlGaAs. [68] There is no known wet etchant for GaN except molten KOH or NaOH [70].

Wet etching is not widely used in industry any more, mainly due to the poor control, potential for contamination, and isotropy. The main problem is that the process is isotropic, so it will undercut the resist layer as it etches vertically. This results in a loss of resolution. The main advantage is that it does not damage the surface and it can be selective, so it can be used for
applications where overetch can be tolerated, but surface damage cannot, such as in opening
dielectric windows for optical devices like photodetectors [69].

3.6.2 Dry Etching

To achieve high resolution pattern transfer, a controlled, anisotropic etch is needed. This is
where dry etching becomes relevant. There are three main types of dry etching: plasma etching,
reactive ion etching (RIE), and high density plasma etching (HDP). Plasma is either a fully or
partially ionized gas composed of equal amounts of positive and negatively charged ions and
some neutral molecules. It is formed when a sufficiently high electric field is applied to a gas to
cause break down and ionization. In the basic plasma etch, the reaction proceeds as follows:
First, the positive ions and free radicals are generated in the plasma, then transported to the
surface of the wafer, followed by adsorption on the surface, reaction, desorption of volatile
products, diffusion into the bulk, and removal through the vacuum system [69].

Plasma chemistry is very complex, and minor changes to the gas mixture can have
significant effects on the etch process. Etching can have both chemical and physical forms. There
is both a chemical reaction taking place to form volatile products that can be desorbed and
removed, but it is also possible to have physical sputtering occurring as well. In general, to
obtain a good plasma etch, producing a reasonable etch rate and smooth surface, one must
balance the chemical and physical etch processes. The earliest plasma etch systems, introduced
in the 1970s, relied on high pressure, low power plasmas. In this process, the etching depends
heavily on the chemistry of the plasma, since it is primarily a chemical process. One of the first
applications was photoresist stripping in an oxygen plasma. Ion milling is the opposite of plasma
etching in that it is a purely physical etch [68].

Reactive ion etching was developed to satisfy the need for anisotropic and selective etch. A
RIE system is a parallel plate reactor operated at a gas pressure of 100-1000 mTorr. This reaction
is essentially chemically enhanced physical etching, and thus physical damage can become a problem. Inductively coupled plasmas (ICP) and other HDP etch systems were developed to improve control over plasma parameters. The advantage of these systems is that the biasing is decoupled, so the wafer is powered independently of the plasma source, so there is less wafer damage. Also, these systems operate at a lower pressure (1-10 mTorr), but high plasma density, so they have high efficiency. These systems provide better critical dimension control, faster etch rates, and improved selectivity [68].

A few common plasma etch gases are: O₂, CH₄, H₂, Cl₂, BCl₃, Ar, and SF₆. A typical RIE/ICP system is equipped with this set of gases, and the gases can be combined. It is as much art as science to understand the plasma chemistry and come up with a gas recipe that will etch a given material well. Typically a matrix of gas flows, pressures, and biases must be investigated to determine the optimum parameters. This set of gases can be used to etch silicon, compound semiconductors, dielectrics, and metals. [68-70] A few typical recipes will be listed in Appendix C.

3.7 Packaging

The packaging process involves dicing the wafer, picking the good devices, and bonding them on chip carriers that can be mounted on circuit boards. This step serves to both protect the chip and interface it with the outside world. A single chip package (SCP) supports a single electronic device, whether it be an integrated circuit (IC), or a simple FET. If multiple active devices are contained in one package, it is referred to as a multi-chip module (MCM). The primary function of the package is to enable the device to perform it’s desired function reliably through the design lifetime of the system [21].

The first package level is the chip to carrier. The wafer carrier serves to decrease wire trace density from the IC level fine pitch of less than 100 um to the typical board pitch of greater than
200 μm. It also serves to encapsulate the chip to protect it from environmental and mechanical stress, and it acts as a heat sink for the chip, providing some level of thermal management. There are three main first-level packaging techniques in the industry: wirebond, tape automated bond (TAB), and flip-chip bond. Wirebonding and flip-chip bonding will be discussed in detail. TAB is used in the LCD industry and involves mounting and interconnecting IC on metallized flexible polymer tape. A schematic of the three packaging schemes is shown in Figure 3-14 [21].

3.7.1 Wire Bonding

Wire bonding is an interconnection technique that involves attaching a fine wire between the I/O pads on the chip and the associated pins on the package. It is widely used in industry and in the early 2000s accounted for over 90% of all chip level interconnections. Typically a gold wire 25 μm thick is bonded ultrasonically between the chip pad and the carrier pin. There are two options for forming the bond: ball bonding and wedge bonding [21].

Ball bonding is a thermosonic welding technique. The primary advantage of ball bonding is that the bond formed is circular, so the wire can be pulled to the next bond in any direction. The bond is formed under a controlled force (<100 g), modest temperatures (150-200 °C), and ultrasonic excitation (60-120 kHz). The wire is then paid out from a spool to form a loop, where the next bond is made. This bond has to be a wedge bond or line fracture since no ball can be formed. After wire fracture, an electronic flame off (EFO) fires to form the next ball bond. Process times can be <20 ms per bond cycle [21].

Wedge bonding is advantageous in fine pitch situations, since the bond wire is only deformed 20-30% beyond the original diameter, compared to 60-80% for ball bonds. It also demonstrates a higher yield, but there is a major drawback: the first bond must be aligned perfectly along the axis between the first and second bonds. Otherwise, the first bond can pull off
if it is moved in a direction off-axis. The bond is formed at a lower temperature (50-125 °C), a controlled wedge bonding force, and ultrasonic excitation. This method essentially applies a force to pinch the wire and the ultrasonic excitation forms the bond [21].

The advantages of wire bonding are the extremely high reliability, ease of automation, and high level of industry infrastructure support. Current automated equipment can bond an entire chip in a fraction of a second. The disadvantages are that it is a serial process so it is an inherently slower bonding process relative to flip-chip, long bond lengths due to the loop of the wire can degrade chip performance, especially for RF packages, there is a larger chip footprint required again due to the wire loop and routing outside of the chip, and there is potential for wire movement and shorting during encapsulation [21].

3.7.2 Flip-Chip Bonding

Flip-chip bonding involves quite literally the face-down direct bonding of the chip pads to the carrier. This method uses solder bump (sphere) interconnections to form both the mechanical and electrical bond, in contrast to wire bonding where an epoxy is used to mount the chip to the carrier and then the gold wires form the electrical connection, with no contribution to mechanical strength. This bonding method is one of the most significant packaging developments to improve cost, reliability, and productivity. There are considerably more processing issues with this method, particularly compatibility between chip pad metallization and solder material and I/O routing issues. Solder bumps are deposited using optical lithography to define the bump pattern and electroplating or evaporation to deposit the metal. After patterning, the bumps are metal posts, and are then reflowed to homogenize the structure, since phase separation can occur during electroplating [21].
The bond is formed by contacting the solder bumps on the chip to the bond pads on the carrier, and heating to the reflow temperature. The solder bumps melt and react with the bond pads, and then the structure is cooled. This is referred to as a controlled collapse interconnection. With the chip facing down, alignment must be performed while the chips are separated. This is accomplished using either a camera with objectives pointing up and down inserted between the components, or with a series of mirrors in an optical microscope. After alignment, the chips are pressed together in a controlled manner, with temperature and force applied. Typical materials are the standard tin/lead (Sn/Pb) eutectic solder for industrial applications. Also of interest due to the low melting point is indium (In) and for MEMS applications where no electrical connection is required, photoresist, such as SU-8, can be used [21].

3.7.3 Encapsulation

Encapsulation of chips significantly enhances reliability of the package, both for wire bonds and flip-chip bonds. It provides both chemical and mechanical protection for the IC. For flip-chip bonded packages, it significantly reduces the strain on the solder bumps, greatly enhancing reliability of the structure. In the case of wire bonded packages, it will seal the wires in place to prevent them from moving or breaking. Moisture is a major contributing factor in packaging failures, so protection from moisture and other chemical attack is critical in electronic packaging [21].

An ideal encapsulant will protect the chip from moisture and chemicals. Mechanical considerations must be kept in mind. It should demonstrate good stress-strain behavior. The coefficient of thermal expansion (CTE) must be close to that of the chip to ensure low stress between chip and underfill. The most common encapsulants fall into four categories: epoxy, cyanate ester, silicone, and urethane. Epoxy is by far the most common encapsulation material. The polymerization process is fast, clean, produces no volatiles, and is very well studies and
established. The other materials are high performance materials for specialized applications. The encapsulation process is typically a simple transfer molding process for wire-bonded packages. Encapsulation of flip-chip packages is accomplished by application around the edge of the chip, and then a capillary force will pull the material under the chip to fill the void [21].

3.8 Board-Level Operations

A printed wiring board (PWB), also called printed circuit board (PCB), is typically a composite of organic and inorganic materials. It contains internal and external wiring, power, and heat sinking. It carries all components of an entire system, so it can also be called a system board or motherboard. It is made of an insulating structure with copper wires both on the surface and in internal layers. Electrical components are soldered on the board to form both the electrical and mechanical connection. FR-4 is the most commonly used composite board material, constructed of multiple plies of epoxy-resin impregnated onto a woven glass cloth. A cross section of a typical PCB is shown in Figure 3-15 [21].

3.8.1 Printed Wiring Board Fabrication

There are two methods of board fabrication: sequential build-up and parallel build-up. The sequential process follows the device chip fabrication process. A series of layers of dielectrics and metals are sequentially deposited and patterned. The parallel build-up process involves fabricating each thin film layer separately, then laminating all layers together. The processes used for PCB fabrication are primarily lithography and etching. Most processing is subtractive, with Cu metal deposited on the board from 10-50 μm thick, followed by lithography with a negative resist and acid etching. An additive process can be used to build thick films, however instead of a lift-off process, a combination of electroless and electrodeposition is used. The electroless plated copper can be used to selectively grow a copper film on the PCB material where there was no copper before. It will selectively grow on windows opened up in the
photoresist, but not on the photoresist itself. This is useful for growing a seed layer 1-5 μm thick. Electrodeposition can be used to build up this layer to be tens of microns thick. Vias can be formed either by etching or physical drilling of the material. Passive components can either be fabricated on the board (inductors from a spiral line, capacitors as two plate between a dielectric layer, and resistors as a line of high resistivity material) or soldered on in the assembly step [21].

3.8.2 Assembly and Testing

PWB assembly is the process is attaching components on the board. Early assembly used through holes to the solder joints on the opposite side of the board from the components. By the early 2000s, nearly 80% of assembly was performed using surface mount assembly (SMA). With this technology, all components are mounted and soldered on one surface. The main advantage of this is a significant reduction in component area, so higher density boards can be fabricated, even putting components on both sides of the board. A schematic showing through hole and surface mount technologies is shown in Figure 3-16 [21].

The main processes for SMA are solder printing, component assembly, and reflow. Solder printing is accomplished using stencil printing. In this process, a squeegee is used to force a bead of solder through a stencil and onto the board. The solder paste usually consists of solder spheres (usually Sn/Pb 63/37), flux (to promote adhesion and remove oxides), and solvent (to adjust viscosity). Chip placement is automated with a camera for alignment, and a vacuum nozzle picks up components and drops them in their locations. For IC chips, a high degree of alignment is necessary due to the relatively small pitch. For passive components, a chip shooter is used, which has high throughput and modest accuracy. This is sufficient since components will self-align to the center of the bond pads during reflow. The reflow step is performed in a multiple zone oven on a moving conveyor. The typical zones include pre-heat, soak, reflow, and cool. There can be
anywhere from 3 to 9 heating zones to finely control temperature and usually a couple cooling zones. The preheat step is to remove the solvent from the solder. The soak phase is to equalize the temperature of all components. The reflow phase is to melt the solder and form the electrical joint, and the cooling phase allows for the solder to solidify before exiting the oven. Control of the temperature profile is critical because this determines the yield, mechanical and electrical integrity, and reliability [21].

Through-hole soldering uses a wave-soldering machine. This type of system solders all components in one pass by passing the board with all components on it across a wave of molten solder where the bottom of the board barely touches the solder. The solder will wet areas of exposed metal, but not areas covered by the top layer of the board, called a solder mask [21].

There is a final test after assembly to ensure functionality. There is actually a test step before each package level. IC testing is performed by the chip manufacturer. This is a simple sort that tests basic functionality. Good chips are packaged and tested again after packaging. PCBs are tested for opens and shorts inside the board, then again after assembly for solder joint continuity. At the system level, more extensive functional testing is performed to make sure the board carries out it’s intended operation [21].

3.9 Reliability

The reliability of a device is the probability that a system will operate within acceptable limits for a given period of time. Since the design lifetime is usually on the order of years to tens of years, accelerated testing must be performed to determine failure rates. Device failure can be caused by thermomechanical, electrical, and chemical mechanisms. An ideal failure distribution follows a “bathtub” curve, shown in Figure 3-17. This implies that at the beginning of the life cycle, there will be a high failure rate, referred to as infant mortality, in which devices fail due to defects introduced in manufacturing. After the initial failure period, there will be a long stable
operation period with few failures. Finally, there will be another period of high failure rate as the devices reach the end of their design life cycle. This curve is referred to as the failure density function, which is the time derivative of the cumulative failure function, which is the fraction of a group of devices that has failed at any given time [21].

The main chemical failure mechanism is corrosion. A physical failure mechanism may be due to creep or other physical aging of polymer encapsulants. Electrical failure can be caused by electromigration. Most failures on the system level are thermomechanical failures. They are caused by packaging stress and thermal expansion coefficient mismatch. This can be manifested in the form of chip cracking, solder joint failure, and delamination. Accelerated testing can be performed to investigate all of these failure mechanisms. Some accelerated tests include: thermal cycling or thermal shock (cycle from -20 °C to 120 °C, for example), thermal soaking (baking for long time), mechanical vibration or applied force (shear applied to solder joints), high voltage or power cycling, and high humidity (environmental chamber at say 90% humidity and 90 °C) [21]. A set of standards has been developed by several different groups, each with different acceptance criteria. The most stringent reliability standards are the US military standards. A more thorough discussion of electrical reliability will follow in Chapter 5.
Figure 3-1. A Czochralski growth system
Figure 3-2. A float-zone refining system

Figure 3-3. A Bridgman furnace
Figure 3-4. Standard flat orientations for Silicon

Figure 3-5. A MBE reactor
Figure 3-6. A MOCVD reactor

Figure 3-7. An ion implantor
Figure 3-8. Positive and negative photoresist patterning
Figure 3-9. Photolysis of DQ upon UV exposure

Figure 3-10. SEM image of a dual layer PMMA-MAA/PMMA resist structure for lift-off
Figure 3-11. An optical lithography system

Figure 3-12. An electron beam lithography system
Figure 3-13. Comparison of pattern transfer via wet and dry etching

Figure 3-14. Schematic of packaging schemes
Figure 3-15. Cross section of a PCB

Through-hole Assembly

Surface Mount Assembly

Figure 3-16. Demonstration of through-hole and surface mount technology
Figure 3-17. Failure density function
CHAPTER 4  
HIGH ELECTRON MOBILITY TRANSISTORS

4.1 Overview

Current work has focused on fabrication of AlGaN/GaN HEMTs on various substrates. As discussed previously, the SiC substrate is of vital importance when heat transfer and high power operation is critical, such as in an application integrating Si-based electronics with GaN. A particularly novel substrate has been demonstrated by Picogiga. It uses a bulk poly-SiC wafer, with a Si layer bonded on the surface, and the GaN grown on the Si. This could potentially integrate the low cost Si approach as a growth template and the high thermal conductivity of SiC. Devices have been fabricated on both substrates, and performance results will be compared in this chapter.

4.2 Silicon Carbide Substrates

SiC substrates are ideal for GaN device fabrication because they offer a thermal conductivity that is more than an order of magnitude higher than sapphire (nearly 400 W/cm-K vs 20 W/cm-K), and a much better lattice match to GaN (3.5% vs 13%). The major drawback is cost. SiC wafers are by far the most expensive (hundreds of dollars per wafer compared to tens of dollars per sapphire wafer), making the devices cost-prohibitive except in high performance markets where extremely high thermal conductivity is a must. Devices fabricated in SiC typically do produce the best performance, and to that end, all devices presented in this section will be compared to SiC devices as a reference [71, 74].

The first section of this chapter will focus on HEMTs fabricated on SiC substrates. As mentioned previously, laser drilling presents an interesting opportunity for novel processing schemes and in particular 3-D integration. Therefore to study the effect of laser drilling on devices, HEMTs were fabricated in a SiC reference sample and a laser drilled SiC sample. For
more details about the laser drilling process, please refer to Chapter 8 of this work. HEMT devices were fabricated on a reference sample as well as a laser drilled sample, both from the same wafer, which had an AlGaN/GaN heterostructure grown by MOCVD on a 4H-SiC substrate by SVT Associates. The laser drilling was performed before HEMT fabrication on an as-received sample. The drilling test, procedures, and characterization is described in Chapter 8.

The first step in processing the HEMT is a dry mesa etch for device isolation. This is performed in an ICP etch for 50 s at 40W RF power and 150W ICP power, using Cl₂/Ar (10 /5 sccm) as the etching gas and a chamber pressure of 2 mTorr (etch rate under these conditions ~ 1000 Å/min). STR-1045 photoresist was used to protect the mesas. A standard ohmic metal scheme (Ti/Al/Pt/Au, 200/600/400/800 Å) was used in a lift-off process using S-1808 photoresist to define the ohmic contacts, which were then annealed at 900 °C in N₂ for 1 minute using rapid thermal annealing (RTA). The ohmic contacts were studied to determine the preliminary effect of laser drilling. The results of this characterization are presented in Chapter 8. The final metal pattern, which supplies the pads for testing and makes the connections to the source, drain, and gate, was patterned and deposited, again in a lift-off process. This metal scheme was Ti/Pt/Au (200/300/3000 Å). The gates were written using e-beam lithography. A special bilayer resist system (7% PMMA-MAA/4% PMMA) was used. The different polymers have different sensitivities to the electron beam, so upon development, there will be an overhanging structure to aid in the lift-off of the Schottky metal (Pt/Au 300/1500 Å). E-beam lithography allows for selective-area gate deposition, as well as submicron gates. These were written to be 250 nm gate length. A device cross-section is shown in Figure 4-1 [71, 74].

Device testing demonstrated nearly identical performance in DC and RF modes on both an undrilled device and on a device fabricated immediately next to a through-hole drilled at 355 nm.
4.3 Silicon On Polycrystalline Silicon Carbide Substrates

SopSiC substrates (Silicon on poly-SiC) are very promising due to the combination of the low-cost approach of silicon and the high thermal conductivity of SiC. While poly-SiC does have a lower thermal conductivity (about 250 W/cm-K) than single crystal SiC, it is still higher than sapphire, GaN, or Si (both 120 W/cm-K). An intriguing approach involves the use of the Smart Cut™ technology already demonstrated in large volume industry (SOI substrates) to produce SopSiC substrates [72-73]. The AlGaN/GaN HEMT wafer is then grown on the silicon on poly-SiC (SopSiC) composite substrate. The thermal conductivity of the composite SopSiC substrate is comparable to that of polycrystalline SiC and superior to Si. For power amplifier applications, ability to extract heat and the allowed thermal budget of operation is critical. High thermal conductivity substrates may make it possible to design a power amplifier without an auxiliary cooling system and lead to further cost savings (materials/operation) along with weight/volume reduction. Thermal simulations of nitride HEMTs operating at power densities of 5–15 W/mm grown on such substrates indicate junction temperatures fairly similar to those of devices on polycrystalline SiC substrates [72-73]. Lastly, good rf quality factors for passive elements such as capacitors, inductors, and transmission lines may be more easily integrated when using high resistivity substrates [73].

The starting substrates were 4 in. diameter high resistivity (111) Si and conducting polycrystalline SiC. The Si was initially oxidized and implanted with a high dose of H ions, cleaned, and bonded to the SiC wafer. Removal of the Si by Smart Cut™ splitting was followed by reclaiming of the top Si wafer and surface preparation of the SopSiC wafer. The SopSiC
wafer consists of the SiC substrate, followed by 0.1 µm of thermal SiO₂, and 0.2 µm of (111) Si. The Molecular Beam Epitaxy (MBE) growth in the rf N₂ plasma-assisted mode of the HEMT structure began with deposition of an ~0.5 µm thick GaN buffer, 1.4 µm additional buffer of Al₀.₂₅Ga₀.₇₅N, and was followed by the active regions of a 100 Å thick GaN channel, then a GaN/AlN 10 period superlattice with total thickness 32 nm and average Al content of 32 at.%, a Al₀.₂₅Ga₀.₇₅N barrier (50 Å) and undoped 20 Å GaN cap layer. The sheet resistance of the HEMT was 456 Ω/sq, with a sheet carrier density of 7 × 10¹² cm⁻² and electron mobility at 300 K of 1400 cm²/V-s. A cross-sectional transmission electron microscopy (TEM) micrograph of the entire structure is shown in Figure 4-6. The structure shows single crystal nature and clean, sharp interfaces, while there is the usual density (~5 ×10⁹ cm⁻²) of threading dislocations originating from the lattice mismatch at the hetero-interface. The ~500 µm thick polycrystalline SiC provides electrical isolation, heat dissipation and mechanical strength. This is followed by ~200 nm of SiO₂ which establishes the quality of the wafer bonding and finally ~470 nm of high resistivity (111) Si which provides a suitable surface for growth of hexagonal GaN and also provides electrical isolation. Device fabrication followed the steps discussed in the previous section for SiC HEMTs, with the exception being that the gate length was written as 0.5 µm in the e-beam lithography system [73].

Figure 4-7 shows a typical I_DS-V_DS characteristics from a HEMT. At top, the device 2x100 µm² gates with 2 µm gate-drain spacing. All of the devices showed excellent gate-drain breakdown voltages in the range 40-350V for gate-drain spacing of 2-125 µm, where the reverse breakdown voltage was defined as the voltage at which the reverse current density was 1µA-cm⁻². These correspond to breakdown fields in the range 3.2-20 ×10⁴ V/cm and are comparable to HEMTs on other substrates with the same sheet carrier density. The maximum drain-source
current of 400 mA was obtained in an 800 µm gate width HEMT, while the highest current density of 375 mA/mm was obtained in the 200 µm gate width devices [74].

We were able to extract the variation in knee voltage as a function of gate-drain spacing from the $I_{DS}-V_{DS}$ characteristics, as shown in Figure 4-8. A minimum value of 2.12 V was obtained for a 2 µm spacing device. This further confirmed the good electron mobility in the two-dimensional electron channel of the HEMT. With the increase of gate drain spacing, the drain resistance and knee voltage proportionally increased. Figure 4-9 shows typical transfer characteristics from a 200 µm gate width device with 2 µm gate-drain spacing. The maximum extrinsic transconductance was $\sim 110$ mS/mm. The maximum intrinsic transconductance was of $143$ mS/mm, which was estimated with

$$\frac{1}{g_{mex}} = \frac{1}{g_{min}} + \frac{1}{R_s},$$

where $g_{mex}$ is the extrinsic transconductance, $g_{min}$ is the intrinsic transconductance and the $R_s$ is the gate-source resistance. The gate source resistance was extracted from the s parameters with an equivalent circuit. The drain current of $\sim 350$ mA/mm is in line with that expected for this sheet carrier density.

One frequently reported problem for AlGaN/GaN HEMTs is that the rf power obtained is still much lower than expected from the dc characteristics [76-81]. This problem is manifested by a collapse in drain current or frequency dispersions in transconductance and output resistance, leading to severely reduced output power and power-added efficiency. Several mechanisms have been identified, including the presence of surface states between the gate and drain which deplete the channel in this region with time constant long enough to disrupt modulation of the channel charge during large signal operation or of trap states in the buffer layer [75-77,80]. Several studies have shown that the use of dielectric passivation layers can be effective in reducing the effects of surface states. We have employed gate lag measurements on surface passivated HEMTs as a metric for establishing the presence of buffer traps [79]. In this method,
the drain current ($I_{DS}$) response to a pulsed gate-source voltage ($V_G$) is measured. Figure 4-10 shows the normalized $I_{DS}$ as a function of drain-source voltage ($V_{DS}$) for both dc and pulsed measurements of a SiN$_X$ passivated HEMT. In the data, $V_G$ was pulsed from –10V to 0 at 0.1MHz and 10% duty cycle. The differences between dc and pulsed drain currents are consistent with the presence of buffer traps. This suggests that further optimization of the buffer growth conditions are necessary.

4.4 Silicon Substrates

GaN on silicon HEMTs are entering commercialization, with Nitronex Corporation offering devices in the 2-4 GHz range. These devices are particularly attractive due to the low cost of the Si substrates (dollars per wafer). Fabrication can prove difficult though, as the lattice mismatch can be difficult to overcome. This factor is offset by the fact that 4-inch Si fabrication process can be easily integrated, wheras SiC and Sapphire are still in the 3-inch wafer level. Si has a moderate thermal conductivity, making it competitive with SiC in all but the highest power markets. GaN on Si is available from Picogiga as well, and some interesting future work could involve a direct comparison of GaN on Si HEMTs and GaN on SopSiC HEMTs.
Figure 4-1. Cross-Section of an AlGaN/GaN HEMT on SiC

Figure 4-2. Image of reference FET (left) and FET adjacent to hole drilled at 355 nm (center, right)
Figure 4-3. I-V Characteristics of reference HEMT (top) and drilled HEMT (bottom)
Figure 4-4. I-V characteristics of reference HEMT (top) and drilled HEMT (bottom)
Figure 4-5. RF characteristics of reference HEMT (top) and drilled HEMT (bottom)
Figure 4-6. Simulation results of junction temperature as a function of substrate.

Figure 4-7. TEM image of SopSiC structure
Figure 4-8. DC I-V curve for SopSiC HEMT

Figure 4-9. DC I-V curve for SopSiC HEMT
Figure 4-10. Pulse curve for SopSiC HEMT
CHAPTER 5
RF RELIABILITY

5.1 Overview

Recently AlGaN/GaN HEMTs have made rapid progress in their characteristics for operation as high power microwave devices due to their excellent properties of high breakdown field of $3 \times 10^6$ V/cm and high sheet carrier density. With this progress, many groups are studying AlGaN/GaN structures intensively for their insertion into applications, such as; for L-band applications including wireless base station of mobile communication systems, for C-band and Ku-band applications on satellite communication systems or fixed wireless access systems. Since AlGaN/GaN HEMTs are able to operate at higher voltage with higher power density than its competitors, the reliability of device at the circumstance of high voltage, high temperature becomes a very critical issue. The degradation mechanisms may be quite different from the conventional III-V GaAs and InP based HEMTs due to the devices operating at a much higher voltage and current region. An example is the phenomena of sudden degradation. In this case, the drain current of the nitride HEMT suddenly increases in the pinched-off condition and reaches failure. To date, there are only limited reports on the long-term reliability of the GaN-HEMTs. However, the commercially available multiple-device reliability test systems are not suitable for the nitride based HEMTs due to high voltage and high power requirements.

There have been sporadic reports, which explain degradation mechanisms with their own unique models [81-86]. Unfortunately, these reports draw conclusions without an adequate amount of lifetime-test data. Multiple channel reliability DC and RF stress test systems are needed to produce enough data for meaningful degradation analysis. We have seen that many issues have an affect on HEMT performance and reliability, including the material quality, strain state, surface cleaning process, and the choice of etch and contact metal scheme.
In device fabrication, we have developed new contact schemes for n-and p-type Ohmic contacts to GaN HEMTs, LEDs and MOS-HEMT gas sensors based on borides. Figure 5-1 shows changes in $I_{DS}$ as a function of time at 350°C for HEMTs with different combinations of Ohmic and Schottky contacts [87]. Devices with conventional Ti/Al/Pt/Au Ohmics show significant decrease in drain current and RF performance over time at 350 °C due to reactions between the GaN and the contact metals. By contrast, the choice of boride-based contacts in addition to use of Pt/Au gate metal show far less change in both DC and RF performance [87-88]. Our newly developed surface cleaning processes combined with improved passivation materials have led to GaN gated MOS-diodes and enhancement mode MOSFETs and superior mitigation of current collapse in HEMTs. Current studies aim to further improve the passivation between source/drain contacts and the gate when the AlGaN is at the surface. This can be accomplished by improved epitaxial growth techniques, device design and passivation.

Traditionally, lifetime prediction for device operation has usually relied on accelerated testing at elevated temperature and then extrapolation back to room temperature operation. This technique frequently fails for scaled, high current density devices found in modern technologies, as shown in Figure 5-2 [89]. Device failure is driven by electric field or current mechanisms or low activation energy processes that are masked by other mechanisms at high temperature. Device degradation can be driven by failure in either active structures or passivation layers [89-91].

5.2 Research Plan – Stress Testing

The research plan for stress testing is as follows. The first test to be performed is RF stress measurements under CW power of 3dB at a Vds of between 30 and 60 V. It has been reported the power degradation has been related to the traps in the buffer layer-within 10 hours of stress, the power degradation could reach 0.5 dB. Second, we will study the stability of gate leakage
current, Imax, gm, and threshold voltage (Vth) - high-temperature (>150 °C) DC 3-terminal aging test in the pinch-off state will be conducted and focused on gate leakage current equivalent to high power operation. Third, we will study the effects of fabrication techniques on current degradation – mesa isolation vs. ion implantation isolation, different Ohmic and Schottky metalliation, Schottky vs. metal oxide semiconductor (MOS) based gate contact, and different passivation approaches will be included in the study. Fourth, we will study the effect of DC operation conditions on the degradation - different drain voltages, drain currents, and junction temperatures will be used in the study. Finally, we will study accelerated life tests performed at elevated temperatures.

Effectively our protocol will be a combination of Si industry-standard approaches and areas specific to compound semiconductors (such as surface passivation and a higher defect concentration). We will run sufficient samples to get decent statistics and determine the lifetime-limiting factors at different temperatures. The usual Arrhenius approach to obtaining operating lifetime from an extrapolation of high temperature data clearly is a problem since mechanisms that occur at high temperature may not really be a factor at lower temperatures. We will use a full range of device and materials characterization methods to better understand the factors determining the reliability of GaN HEMT technology. Failed devices can be analyzed to determine if macroscopic defects (dislocations) have played a role in the device break down. We largely have these capabilities in house so we can provide quick turnaround on device fabrication.

5.3 Stress Test System

A block diagram of a single frequency 32-channel test system is shown in Figure 5-3. The system we are going to build consists of 4 RF driver boards with an output to 2-way splitters,
creating 8 outputs at approximately 5 W each. A voltage-controlled oscillator is used to synthesize the RF signal, then a series of amplifiers and attenuators is used to tune the output to the required power level, shown schematically in Figure 5-4. The splitter boards have isolators, directional couplers, and diode detectors to detect both forward and reflected power as an output voltage, detailed in Figure 5-5.

The signal then goes into the device boards. These have the input and output matching networks fabricated on the circuit board or integrated on the GaN chip, with a thick copper layer on the back side for heat sinking and as a common ground plane. A hole is bored through the boards to the copper for the device cavity. The device is mounted directly on the copper using Diemat, and wire bonded, as shown in Figure 5-6.

This pre-matched circuit board is designed as disposable board. On the back side of the board, thermoelectric heaters are clamped on with a thermostat for temperature sensing. This allows for temperature control. The heaters will be controlled by PID controllers with a computer interface. The device boards also have DC control and monitoring capabilities. The RF output from the boards goes to a detector diode board. The diode detectors work by rectifying the RF signal into a DC voltage output. This output must be calibrated since the response will be different at different frequencies. This can be done by using a synthesized sweeper to input a known power to the diode, and simply measuring the output with a digital multimeter. A curve can then be fit to this data and an equation and constants extracted, as shown in Figure 5-7. We have performed the thermal simulations of the HEMT for different power levels and device configuration. The HEMT junction temperature can be easily higher than the physical device by more than 100 °C [92-93]. It is very important to determine the junction temperature during the
reliability test. We propose to acquire a thermal image system to determine the actual junction temperature during the stress measurements.

This equation can be input to LabView to perform the direction during acquisition. All control and acquisition is processed in LabView. A full summary of the data that is processed is as follows. DC source/drain bias and gate bias, RF generator output power, and temperature are controlled. DC source/drain bias and gate bias, RF forward and reverse input power, RF output power, and temperature are monitored and plotted as a function of time in LabView while acquiring data. The data acquisition summary is shown in Figure 5-8.

The modular approach we have taken allows for considerable flexibility and expandability to the system. Additional test capacity can be added on down the road, and the frequency of the system can be changed by simply changing the driver components. Most importantly though, the independent device test boards can be easily changed out to accommodate any type of device, so both packaged devices and bare die can be tested by simply redesigning the test board. This also then does not limit the system to purely nitride device testing. The system can be used to test any device so long as the board is designed with the proper matching components.
Figure 5-1. Changes of $I_{DS}$ as a function of time at 350°C for HEMTs with different combinations of Ohmic and Schottky contacts.

Figure 5-2. RF power output as a function of time
Figure 5-3. A single frequency 32 channel RF and DC reliability test stand

Figure 5-4. The RF source
Figure 5-5. The splitter board

Figure 5-6. A pre-matched circuit board
Figure 5-7. Calibration and curve fitting of a diode detector.

Figure 5-8. Data acquisition.
CHAPTER 6
GAS SENSING

6.1 Overview

There is significant interest in developing GaN diodes for gas sensor applications. The gate region can be functionalized so that current changes can be detected for a variety of gases, liquids, and biomolecules. Hydrogen sensors are particularly interesting with the emerging fuel cell vehicle market. The use of simple Schottky diode structures using thin Pt contacts allows for detection of hydrogen at concentrations of hundreds of ppm at wide temperature range temperatures (room temperature-500°C) [105-114]. There are also applications for detection of combustion gases for fuel leak detection in spacecraft, automobiles and aircraft, fire detectors, exhaust diagnosis and emissions from industrial processes [105-110].

Simple two-terminal semiconductor Schottky diodes with Pt or Pd gates have been shown to be particularly effective hydrogen sensors. A cross section schematic and an optical image of a Schottky diode sensor is shown in Figure 6-1. Typically the sensing mechanism is ascribed to the dissociation of the molecular hydrogen on the Pt gate contact, followed by diffusion of the atomic species to the oxide/semiconductor interface where it changes the piezo-induced channel charge and effective barrier height on Schottky diode structures. This effect has been used in Si, SiC, ZnO and GaN–based Schottky diode combustion gas sensors [94-109]. Three-terminal transistor structures have been investigated to a much less extent but may have advantages because of the presence of the capability for current gain. AlGaN/GaN HEMTs are an attractive option as the hydrogen sensor because they can operate over a broad range of temperatures and form the basis of next-generation microwave communication systems so an integrated sensor/wireless chip is possible [115-116].
6.2 Hydrogen Sensors

6.2.1 Gallium Nitride High Electron Mobility Transistor Sensors

AlGaN/GaN Schottky diodes with Pt sensing metal demonstrate improved sensitivity under reverse bias and elevated temperature. A detection limit of 10 ppm was achieved under reverse bias with a current increase of 14%. The detection limit was further decreased to 1 ppm by operating the sensor at 150 °C, still demonstrating a current change of nearly 50%. This is a considerable improvement over the forward bias detection limit of 100 ppm, with a current change of 4% [117].

The device layer structures were grown on C-plane Al2O3 substrates by Metal Organic Chemical Vapor Deposition (MOCVD). The layer structure included an initial 2μm thick undoped GaN buffer followed by a 35nm thick unintentionally doped Al0.28Ga0.72N layer. Mesa isolation was achieved by using an inductively coupled plasma system with Ar/Cl2 based discharges. The Ohmic contacts were formed by lift-off of Ti (200Å)/Al (1000Å)/TiB2 (200Å)/Ti (200Å)/Au (800Å). The metals were deposited by Ar plasma-assisted RF sputtering. The contacts were annealed at 850 °C for 45 sec under a flowing N2 ambient in a Heatpulse 610T system. A 100 Å thick Pt Schottky contact was deposited by e-beam evaporation for the Schottky metal. The final step was deposition of e-beam evaporated Ti/Au (300Å/1200Å) interconnection contacts. The individual devices were diced and wirebonded to carriers. These were then placed in an environmental test chamber and connected to an electrical feedthrough for testing. Mass flow controllers were used to control the gas flow through the chamber, and the devices were exposed to either 100% pure N2, or H2 concentrations of 500 ppm down to 1 ppm in N2 and temperatures from 25 to 500 °C [117].
Devices were tested under both forward and reverse bias conditions at room temperature (25°C) in a nitrogen atmosphere. There was an increase in current under both forward and reverse bias conditions upon exposure to hydrogen, as shown in Figure 6-2. This is consistent with previously discussed mechanisms in which the hydrogen molecules dissociate into hydrogen atoms through the catalytic action of the Pt gate contact, and diffuse to the Pt/AlGaN interface [96-97, 102, 106, 109, 118-123]. The hydrogen atoms form a dipole layer, lower the Schottky barrier height, and increase net positive charges on the AlGaN surface as well as negative charges in the 2DEG channel. The calculated barrier height decrease for 500 ppm and 100 ppm hydrogen is 5 meV and 1 meV, respectively. The ideality factors were calculated to be 1.25 and 1.23 in 500 and 100 ppm hydrogen, respectively, compared to 1.26 in 100% nitrogen [117].

However, a plot of hydrogen sensitivity (defined as the drain current change over the initial drain current) versus bias voltage shows different characteristics for forward and reverse bias polarity conditions at 500 ppm of H₂, as shown in Figure 6-3. For the forward bias condition, there is a maximum sensitivity obtained around 1 V and further increase of bias voltage reduces the sensitivity. The sensitivity for the reverse bias condition is quite different and it increases proportionally to the bias voltage. We propose the following mechanism for the change in sensitivity under forward and reverse bias conditions: (1) The initial increase in the sensitivity is due to the Schottky barrier height reduction. (2) Further increase in forward bias allows electrons to flow across the Schottky barrier. These excess electrons bind with H⁺, form atomic hydrogen, and gradually destroy the dipole layer at the interface, therefore losing the hydrogen detection sensitivity. (3) For the reverse bias condition, electrons given away by the hydrogen atom may be swept across the depletion region. At higher reverse bias voltage, a
higher driving force is applied to the electrons to move across the depletion region. Thus the dipole layer is amplified at the Pt/AlGaN interface for higher reverse bias voltage. Due to this dipole layer amplification, the detection sensitivity is enhanced at higher reverse bias voltage. The change in current upon exposure to hydrogen is directly related to the hydrogen concentration, as demonstrated in Figure 6-4, where current was monitored as a function of time, with the hydrogen concentration being increased from 1 ppm to 500 ppm, alternating between hydrogen and nitrogen exposure [117].

It is also evident in Figure 6-5 showing the detection sensitivity as a function of hydrogen concentrations, that the diodes are much more sensitive under reverse bias conditions. A detection limit of 100 ppm is achieved under forward bias, but the reverse bias detection limit is an order of magnitude lower, 10 ppm. The change in current at 10 ppm is 14% and over 200% at 500 ppm under reverse bias conditions. This demonstrates again that the same sensor under reverse bias has a much lower detection limit, as forward bias operation results in changes of 25-75% over the 100-500 ppm range. This is consistent with published reports indicating improved sensitivity under reverse bias [124]. The reliability of the hydrogen sensor may be quite different under the two bias voltage polarities, since different degradation mechanisms in GaN devices are accelerated by either the presence of high voltage depletion regions (reverse bias) or current injection (forward bias in this experiment) [89].

Temperature effects were studied next. A hydrogen concentration of 25 ppm was chosen to study the temperature effects since it demonstrated a large response at room temperature. The diode current was measured in both 25 ppm H\textsubscript{2} and 100\% N\textsubscript{2} atmospheres at temperatures from 25 °C to 500 °C. The percentage change in current as a function of temperature is shown in Figure 6-6. At temperatures above 550 °C, the device was irreversibly damaged. It is interesting
to note the peak in the response at around 200 °C. This is due to competing effects on the surface. It is expected that with increasing temperature, the cracking of the hydrogen on the surface will become more efficient. This will result in more molecular hydrogen, which will also diffuse to the metal-semiconductor interface faster at increased temperature. This effect is countered by basic kinetics. There will also be a decreased surface concentration of hydrogen, since there will be more transport to and from the surface at elevated temperature.

With this in mind, studies were performed to see if even lower detection limits were possible under elevated temperature conditions. A temperature of 150 °C was chosen since it demonstrated a large response without pushing the temperature so high that the device was damaged. As shown in Figure 6-7, a repeatable detection limit of 1 ppm was observed. Given the relatively large response even at 1 ppm, there is speculation that even lower detection limits can be achieved, but 1 ppm was the limit of the testing system.

6.2.2 Wireless Hydrogen Sensor Network

We have demonstrated a wireless hydrogen sensing system using commercially available wireless components and GaN Schottky diodes as the sensing devices. Our sensors have achieved ppm level detection, with the added advantages of a very rapid response time within a couple of seconds, and rapid recovery. The sensors have shown current stability for more than 8 months in an outdoor environment. Our wireless network sensing system enables wireless monitoring of independent sensor nodes and transmits wireless signals. This is especially useful in manufacturing plants and hydrogen-fuelled automobile dealerships, where a number of sensors, possibly with each detecting different chemicals, would be required. We have also developed an energy-efficient transmission protocol to reduce the power consumption of the remote sensor nodes. This enables very long lifetime operation using batteries. Experimental
results showed that a 150 meter transmission distance can be achieved with 10 mW total power consumption. The entire sensor package can be built for less than $50, making it extremely competitive in today's market [115-116].

The sensor devices are based on the technology described in the previous section, and demonstrate comparable characteristics. An instrumentation amplifier is used for the detection circuit to sense the change of current in the device. The current variation, embodied as a change in the output voltage of the detection circuit, is fed into the microcontroller. The microcontroller calculated the corresponding current change and controlled the ZigBee transceiver to transmit the data to the wireless network server. The block diagram of the sensor module and the wireless network server are shown in Figure 6-8 [115-116].

The Zigbee compliant wireless network supports the unique needs of low-cost, low-power sensor networks, and operates within the ISM 2.4 GHz frequency band. The transceiver module is completely turned down for most of the time, and is turned on to transmit data in extremely short intervals. The timing of the system is shown in Figure 6-9. When the sensor module is turned on, it is programmed to power up for the first 30 seconds. Following the initialization process, the detection circuit is periodically powered down for 5 seconds and powered up again for another 1 second, achieving a 16.67% duty cycle. The ZigBee transceiver is enabled for 5.5ms to transmit the data only at the end of every cycle. This gives a RF duty cycle of only 0.09% [115-116].

A web server was developed using MATLAB to share the collected sensor data via the Internet. The interface of the server program, shown in Figure 6-10, illustrates three emulated sensors with different baseline currents. If any of the sensor’s current increases to a level that indicates a potential hydrogen leakage, the alarm would be triggered. A client program was also
developed to receive the sensor data remotely. As shown in Figure 6-10, the remote client was able to get a real time log of the system for the past 10 minutes via the client program. In addition, a full data log obtained via accessing the server via a ftp client as the server program incorporates a full data logging functionality. When an alarm was triggered, the client was able to deactivate the alarm remotely by clicking a button on the interface. The server program for the wireless sensor network could also report a hydrogen leakage emergency through phone line. When the current of any sensors exceeded a certain level, indicating a potential hydrogen leakage, the server would automatically call the phone-dial program, reporting the emergency to the responsible personnel [115-116].

The sensor module was fully integrated on an FR4 PC board and packaged with battery as shown in Figure 6-11 (a). The dimension of the sensor module package was: 4.5 × 2.9 × 2 inch³. The maximum line of sight range between the sensor module and the base station was 150 meters. The base station of the wireless sensor network server was also integrated in a single module (3.0 × 2.7 × 1.1 inch³) and ready to be connected to laptop by a USB cable, as shown in Figure 6-11(b) and (c). The base station draws its power from the laptop’s USB interface, thus do not require any battery or wall transformer [115-116].

Field tests have been conducted both at University of Florida and at Greenway Ford in Orlando, FL. The setup at Greenway Ford was aimed to test the stability of the sensor hardware and the server software under actual operational environment. Two sensor nodes were installed and the test was started on the 30th of August 2006. Six sensor modules and the server have been functioning to date [115-116].

The outdoor tests at University of Florida have been conducted for several times, to test the sensor’s response to different concentrations of hydrogen at different distances. The tested
hydrogen concentrations include: 1%, 4%, and 100%, and the distance from the outlet of hydrogen to the sensor ranges from 1 foot to 6 feet. Hydrogen leakage was successfully detected for all these cases, triggering the program to send alarm to cell phone. Figure 6-12 shows the test result with four running sensor modules and 4% hydrogen at 3 feet away from the hydrogen outlet. The sensors were tested sequentially so the effects of each sensor can be isolated. The test results also display the reliability of the wireless network as it is able to collect the data from each individual sensor.

Initial results of field testing indicated that reliability of the sensors could be a concern, as the single diode sensors showed a periodic rise and fall in the current level, which can be attributed to a temperature effect. This is shown in Figure 6-13. There was also a long term current degradation, which was attributed to ohmic contact degradation within the device due to the continuous bias. As a result, TiB$_2$-based ohmic contacts have been employed, which have been proven to improve stability for long term operation [125]. To avoid the thermal effects, the sensing device was redesigned to employ a differential detection scheme. This involved a reference diode, which is encapsulated, and an active diode, which is open to the ambient. Detection is achieved by monitoring the difference in current between the two devices as opposed to measuring an absolute current level. Test results demonstrating the operation of the device are shown in Figure 6-14. It is demonstrated in this figure that at room temperature and elevated temperature, the reference diode does not show a current change upon exposure to hydrogen, while the active diode does. The combination of differential diode sensors and boride-based ohmic contacts has significantly improved stability and reliability. Recent field data is shown in Figure 6-15, and the data can be monitored in real-time at the following website: http://ren.che.ufl.edu/app/realtimeSensing.htm [115-116].
Figure 6-1. A Schottky diode hydrogen sensor shown in cross-section (top) and optical image (bottom)
Figure 6-2. Forward and reverse bias plot of diode current in varying atmospheres

Figure 6-3. Percentage change in current as a function of bias at 500 ppm H₂
Figure 6-4. Time dependence of Schottky diode sensor when switching from pure nitrogen atmosphere to hydrogen concentrations from 1-500 ppm

Figure 6-5. Percentage change in current as a function of hydrogen concentration under both forward and reverse bias.

\[ V_{\text{Reverse}} = -3.5 \text{ V} \]
\[ V_{\text{Forward}} = 1.0 \text{ V} \]
Figure 6-6. Percentage change in current as a function of temperature at a hydrogen concentration of 500 ppm.

Figure 6-7. Time dependence of Schottky diode sensor when switching from pure nitrogen to 1 ppm hydrogen under reverse bias at 150 °C
Figure 6-8. Block diagram of sensor module and wireless network server

Figure 6-9. System timing of at wireless sensor node

Figure 6-10. Interface of online hydrogen level monitoring
Figure 6-11. Photo of sensor system (a) Sensor with sensor device; (b) Sensor and base station; (c) Computer interface with base station

Figure 6-12. Field test results of four sensors

Figure 6-13. Field test results for single diode sensors over a period of one week
Figure 6-14. Differential diode test results using 1% H$_2$ at room temperature and elevated temperature

Figure 6-15. Field test results over a month period for differential diode sensors with boride-based ohmic contacts
7.1 Overview

GaN-based devices are optimal for high power, high temperature, and high speed applications. Silicon dominates the low power, low frequency IC market with CMOS technology. A new hybrid approach involves vertically integrating GaN and Si devices to obtain the best performance from both devices. A design investigated in this work involves the integration of a Si modulator chip and a GaN power amplifier (PA) in a vertical stack, with a heat sink on top integrated with the antenna. Thermal management is critical in such a design since Si device are much more sensitive to temperature and cannot operate reliably above 150-180 °C. The integration of these two types of devices must, therefore, be optimized for heat transfer to efficiently draw the heat from the GaN device before it affects the performance of Si devices.

A first-generation schematic of the MCM 3-D integration of GaN and Si components on high resistivity Si is shown in Figure 7-1. The Si modulator chip and GaN PA chip are flip-chip bonded, providing room for expansion to include more circuits and functions. The ideal vertical stack design is shown in Figure 7-2. The Si modulator is bonded to the common ground plane and GaN PA chip using polydimethylsiloxane (PDMS). The PDMS layer also has a secondary function as a thermal insulator for the Si modulator, due to the low thermal conductivity (~0.1 W/m-K). In the real package, metal vias would be added to make the electrical connections between chips and to the common ground plane.

7.2 Finite-Element Modeling

To study heat transfer through the package, finite-element modeling was used to look at various parts of the package. This method breaks down the actual geometry into a mesh, which is
an interconnected system of nodes, with averaging occurring in the space between the nodes. The physical differential equation governing the variable of interest is applied at each node, creating an enormous system of equations. The equations are solved simultaneously and the results plotted. The particular advantage of this method is that it can solve differential equations in geometries that defy analytical solutions because the mesh is essentially a breakdown of the geometry into a number of connected linear regions. To that end, by enabling a finer mesh, one is able to achieve more accurate results, but considerably more computing power is required.

By performing a finite-element analysis using FlexPDE software, a package design to optimize heat transfer could be realized. A brief discussion of heat transfer principles will begin this section to allow for a better understanding of the simulations performed. From there, multiple generations of simulations will be discussed and results presented.

7.2.1 Heat Transfer

There are three modes of heat transfer: conduction, convection, and radiation. Energy transfer through conduction is accomplished through direct molecular collisions and through free electrons. The ability of any given material to conduct heat is referred to as thermal conductivity, k, and is analogous to electrical conductivity. Conductive heat transfer at steady state is described by Fourier’s first law of heat conduction, also known as the Fourier rate equation, shown below. It is analogous to the molecular momentum transfer equation [126].

\[
\frac{q}{A} = -k \nabla T
\]

The thermal conductivity is independent of direction, and is primarily a function of temperature and is a fundamental physical property of a conducting medium. Depending on the material, it can be considered constant over a modest temperature range.
Convective heat transfer involves energy exchange between a surface and adjacent fluid. Natural convection occurs when there are no external forces driving the fluid, just the natural circulation due to density differences in the fluid from temperature variation. Forced convection occurs when there is an external driving force such as a pump or fan. Convective heat transfer is described by Newton’s law of cooling, also known as Newton’s rate equation [126].

\[
\frac{q}{A} = h\Delta T
\]

In this equation, \( h \) is the convective heat transfer coefficient. It is not a constant and generally is a function of system geometry, fluid, flow properties, the difference in temperature, and the type of convection present.

Radiative heat transfer occurs between two surfaces and does not require a medium to propagate. This is the only method of heat transfer in a vacuum. The energy emission by a perfect radiator (black body) is given by the Stefan-Boltzmann law of thermal radiation [126].

\[
\frac{q}{A} = \sigma T^4
\]

This equation must then be corrected for deviations from black body behavior. It is common for all three methods of heat transfer to be taking place simultaneously. For this work, the effects of radiative heat transfer are minimal compared to conduction and convection. Consider as an example a situation where a hot gas is contacting a 3-material composite wall, with a cold gas on the other side. The heat transfer can be described as a series sum of convective heat transfer between the hot gas and the first surface, conduction through the first material of thermal conductivity \( k_1 \), conduction through the second material of thermal conductivity \( k_2 \), conduction through the third material of thermal conductivity \( k_3 \), and convection again at the wall. This is shown schematically in Figure 7-3. Considering these walls
ot be infinite in the y and z directions, we can solve the Fourier equation in the x-direction by integrating with the boundary conditions $T(x=0)=T_1$ and $T(x=L)=T_2$ to obtain the result below [126].

$$q = \frac{kA}{L} \Delta T$$

This resembles Newton’s rate equation. Since the system is at steady state and no heat is generated or destroyed, the heat transfer through each layer must be equal. Therefore the total heat transfer can be written by equating each term:

$$q = h_A(T_h - T_1) = \frac{k_A}{L_1}(T_1 - T_2) = \frac{k_A}{L_2}(T_2 - T_3) = \frac{k_A}{L_3}(T_3 - T_4) = h_A(T_4 - T_c)$$

This can be rearranged to determine the total change in temperature:

$$T_h - T_c = q \left( \frac{1}{h_A} + \frac{L_1}{k_A} + \frac{L_2}{k_A} + \frac{L_3}{k_A} + \frac{1}{h_A} \right)$$

From this equation, one can see that heat transfer can be described in a manner analogous to Ohm’s law for electrical circuits. This gives rise to the term thermal resistance, where $R=1/hA$, $L/kA$. This example is shown as the equivalent of a series circuit. One can imagine a geometry including materials in parallel, which would produce an equation similar to a parallel circuit. The equation can be generalized in an analogous manner to Ohm’s Law with an equivalent thermal resistance instead of electrical resistance [126]:

$$q = \frac{\Delta T}{R_{T,\text{Eq}}}$$

$$R_{T,\text{Eq}} = \Sigma R_{T,i}$$

By performing an energy balance on a given control volume of dimension $\Delta x$, $\Delta y$, and $\Delta z$, it is possible to obtain a transient differential equation for general heat transfer. This equation can be written as follows in the limit as $\Delta x$, $\Delta y$, and $\Delta z$ approach zero [126]:
\[ \nabla \cdot k \nabla T + q + \Lambda = \rho c_v \frac{DT}{Dt} + \nabla \cdot \mu \nabla v \]

In this equation, \( q \) refers to the total energy generation, \( \Lambda \) refers to the viscous work rate per unit volume, and potential and kinetic energy terms are simplified in the right hand side of the equation. From here, the equation can be further simplified for the purposes of the simulation by taking the case where there is no fluid motion and all heat transfer is by conduction. This equation, which is the one used in the thermal simulations, can be written as follows [126]:

\[ \rho c_p \frac{DT}{Dt} = k \nabla^2 T + q \]

In this case, \( T \) is the temperature, \( t \) is time, \( \rho \) is density, \( C_P \) is the heat capacity, \( k \) is thermal conductivity (W/cm-K), and \( P_D \) is the dissipated power (generated in the device). The latter can be determined from the product of bias voltage and drain current through the HEMT, divided by the HEMT layer volume [126].

To solve the differential equation, boundary conditions must be specified. The initial conditions refer to the values at the start of the time period of interest. For this equation, temperature is the only variable, and therefore the initial condition can be considered to be room temperature. The boundary conditions refer to the values of the variable of interest at the system boundaries. There are three types of boundary conditions for this type of problem: isothermal boundary, which is a constant temperature (\( T = \text{const} \)), insulated boundary, where there is no heat flow across the boundary (\( dT/dx = 0 \)), and boundaries with a function describing the temperature. This type of boundary is typically described by a change in the method of heat transfer, such as conduction transferring heat to a surface and convection removing heat at the surface. This can be written as follows, assuming a convective heat transfer coefficient and temperature far from the surface as \( T_{\text{inf}} \) [126]:

110
\[ h_{\text{surf}} (T_{\text{surf}} - T_{\text{inf}}) = -k \left( \frac{\partial T}{\partial x} \right) \]

Perhaps the most difficult part of the simulation is setting up the boundary conditions to be realistic. For this work, convective boundary conditions were typically used because it is the most realistic case (the package will operate in air, not in an insulated or isothermal environment, thus there will be convective heat transfer at the boundary). The major problem with convective boundaries is the convective heat transfer coefficient, \( h \). Given that \( h \) is usually a function of temperature and geometry, it can be very difficult to determine a reasonable value to use in the problem, and empirical measurements are typically used to calculate a value. There are a number of correlations available for calculation of \( h \), which are typically empirically fitted functions of various dimensionless groups, defined below [126]:

\[
Nu = \frac{hL}{k}
\]

\[
Pr = \frac{\mu c_p}{k}
\]

\[
Gr = \frac{\beta g \rho^2 L^3 \Delta T}{\mu^2}
\]

\[
Ra = Gr \ Pr
\]

\[
Pe = Re \ Pr
\]

One must pay careful attention to the conditions where each case is valid. Perhaps the best correlation for natural convection is the Churchill and Chu correlation. It is used for flow over vertical plates and shows good results over 13 orders of magnitude of the Rayleigh number (Ra). The Ra number is defined as the product of the Grashof number (Gr) and Prandtl number (Pr) [126].
For forced convection, there are many more correlations, some describing laminar flow and some describing turbulent flow, and the many different regimes of each. For laminar flow, the Sieder-Tate correlation provides very good results for flow through pipes, and the Dittus-Boelter generally gives good results for turbulent flow under common conditions \[126\].

\[
Nu = \left\{ 0.825 + \frac{0.387Ra^{1/6}}{1 + \left( \frac{0.492}{Pr} \right)^{9/16}} \right\}^2
\]

Note that most correlations are calculated for fluid flow through pipes or for flat surfaces. The heat sink design for this simulation provides an interesting geometry, as the stacked fins of a heat sink cannot be considered independent infinite plates or enclosed pipes for fluid flow purposes. Furthermore, heat sinks typically have a fan blowing over them to improve heat transfer. This creates a forced convection case, where a free-standing heat sink would present a natural convection case. To this end, rather than using the true dimensions of the heat sink, one can use the hydraulic diameter as a substitute for length or diameter in the calculations above. It is defined as a ratio of surface area to perimeter as follows \[127\]:

\[
D_h = \frac{4A}{P}
\]

This length quantity is useful in situations where the equations are solved using perfectly circular geometries, but the actual geometry is elongated. One could view the area between the fins of the heat sink as elongated channels. An alternative would be to determine the value
experimentally by machining a custom heat sink, putting a thermocouple on the top surface, a thermocouple and heat source on the bottom surface, and therefore knowing \( Q \), \( A \), and \( \Delta T \), one can back out \( h \) from the convective heat transfer equation [127].

### 7.2.2 First Generation Simulation: GaN Power Amplifier on Heat Sink

As an initial test of the model, a simplified system was studied. This system consisted of a GaN HEMT on the heat sink. This structure resembles the schematic for the first generation device. Figure 7-4 shows a schematic of the device centered on the integrated heat sink/antenna. The assumed initial values were: 3 W/mm dissipated power in the GaN power amplifier, a 5 \( \mu \)m thick GaN layer, 500 \( \mu \)m thick SiC layer, and an effective convective heat transfer coefficient, \( h \), of 30 W/m\(^2\)-\( ^\circ \)C. The heat sink was assumed to be \(~20 \text{ mm}^2\) area, with 11 fins, 10 mm fin height, and 0.94 mm fin width, which are the dimensions required for a 2.4 GHz antenna. The finned heat sink acts as a large thermal mass for heat removal. From these starting values, each layer was optimized by systematically varying the thickness to find the minimum steady state temperature. The most realistic boundary condition is a convective boundary on all sides [92-93].

The first variable studied was thermal conductivity. This is manifested in the design in the substrate selection. Figure 7-5 shows the expected maximum temperatures reached by the integrated power amplifier and modulator at fixed power and layer thickness for different substrates. Clearly the use of sapphire substrates is not an effective solution because of their poor thermal conductivity. The resultant high device temperature would be a major detriment to the reliability of the GaN power amplifier in particular, since it is very difficult to prevent reaction of the gate metal at 400 \( ^\circ \)C during extended operation. The surprising result from Figure 7-5 is that use of a bulk GaN substrate, while still inferior to SiC, would still maintain the die temperature
at less than 200 °C at 3 W/mm. Of course, the optimal substrate is single crystal SiC, with the highest thermal conductivity [92-93, 128-131].

The thickness of the substrate also plays an important role in the thermal characteristics of the MCM. Figure 7-6 shows that, for a SiC substrate, if the substrate is thinned down from the usual 600 μm to 100 μm, there is an improvement of ~50 °C in the operating temperature of the chip at a fixed PA power of 3 W/mm. This is due to lowering of the thermal resistance by thinning down the chip; however, there is also a slight rise in operating temperature below 100 μm. Once the substrate becomes too thin, there is an increase in the lateral thermal resistance, which will drive up the junction temperature. These are important considerations when designing the interconnect vias. The dry etch rates of SiC are usually below 1 μm/min and, thus, the SiC substrate is often thinned down to reduce the etch time for via hole formation; therefore, 100 μm would be an optimal substrate thickness [92-93].

Figure 7-7 shows the effect of PA power density on the temperature rise of the MCM, assuming a standard thickness SiC substrate with no vias or wires in the structure for simplicity. At high power levels even the use of a SiC substrate is unable to keep the MCM from reaching 400 °C at 10 W/mm. The GaN PA can theoretically operate at this temperature if it uses thermally stable metallization, but the Si modulator would be inoperable. The PA operating temperature can be reduced to below 200 °C even at 10 W/mm by optimizing the substrate thickness as discussed above and shown in Figure 7-7. The design of the device also plays an important role, and using a fingered design, consisting of 4 gates with 250 μm gate width, provides an improvement of ~50 °C over a single gate with 1 mm gate width [17-19, 92-93, 131-132].
Free convection is the only heat dissipation mechanism through the outer vertical-surface of the MCM. The amount of heat dissipation through free convection is five orders smaller as compared to the conduction through the integrated heat sink antenna. The thermal resistance at the convective boundary is $\sim 85 \, \text{K/W}$, compared to $\sim 2 \times 10^{-4} \, \text{K/W}$ for conduction through the package. Therefore, the temperature rise at the center of the chip on the top surface was highest (around $\sim 110 \, ^\circ\text{C}$), and there was a $\sim 40 \, ^\circ\text{C}$ difference between the center and edge of the structure, based on a power amplifier density of 3 W/mm. To investigate the temperature rise while the device is turning on, the transient equation was used. The temperature profile reached steady state in the range of $\sim 30 \, \text{sec}$ [92-93].

Other MCM design considerations that were also considered, but were not found to have a significant effect on the operating temperature, were the GaN epi-layer thickness ($\sim 5 \, ^\circ\text{C}$ difference for 10 $\mu$m versus 3 $\mu$m) and the wire thickness and length ($\sim 2-8 \, ^\circ\text{C}$ difference for wire lengths from 2-100 mm and thicknesses of 0.2-10 $\mu$m) [92-93].

7.2.3 Generation II: Combined Amplifier and Silicon Chip

After initial study and optimization of heat transfer through the GaN PA on the heat sink, it is logical to go back and consider the more complex problem of modeling the entire 3-D package. The optimized GaN PA parameters were used as starting points for this work: 3 W/mm dissipated power in the GaN power amplifier, a 2 $\mu$m thick GaN layer, 100 $\mu$m thick SiC layer, and an effective convective heat transfer coefficient, of 30 W/m$^2$-°C. The heat sink was, again, assumed to be $\sim 20 \, \text{mm}^2$ area, with 11 fins, 10 mm fin height, and 0.94 mm fin width. The additional layers added in a vertical stack to complete the 3-D structure were the PDMS layers for bonding (4 $\mu$m each), an Au common ground plane (5 $\mu$m), and the Si modulator chip (500 $\mu$m) [92-93].
Figure 7-8 shows the expected maximum temperatures reached by the power amplifier for various Si layer thickness and fixed power density of 3 W/mm. The effect is small, changing by only approximately 10 °C over an order of magnitude thickness range. Therefore, standard thickness Si substrates can be used for the modulator device without incurring any substantial losses in thermal management. It would be beneficial however, cost permitting, to use thin Si membranes for the modulator, using PDMS as a chip carrier. This could prove essential technology if this extra 10 °C drop will make the difference between the function and failure of the Si devices, since these are the most temperature-sensitive component in the MCM [92-93].

The typical temperature distribution in both GaN and Si layers is shown in Figure 7-9. The Si temperature distribution is considerably broader, due to lateral spreading from the high thermal resistance PDMS layers. This effect is highlighted in Figure 7-10, which shows a typical cross sectional temperature distribution in various layers in the device. Note from the scale that this shows only a small area, 2.5 mm on either side of the gate. The temperature in all layers reaches the same value within 2 mm of the gate, and is sharply peaked in the GaN layer, becoming broader down through the Au and Si layers, with the PDMS layers spreading the heat. The effects of both PDMS and Au thickness were also studied, and the effect over a range of 15 μm was negligible (<3 °C) [92-93].

After optimization of all layer thicknesses in the structure, the device power level was studied. Previous work had shown that optimization of the GaN device design could drive down the high power operating temperature considerably from a reference case. Now, due to the high thermal resistance from the PDMS layers, the junction temperature of the HEMT rises again to 350°C at high power levels, even with all layers optimized, as shown in Figure 7-11. Again, the GaN PA can operate at this temperature, but the Si modulator would be inoperable, even with
thermal insulation. It is, therefore, logical to attempt to drive down the operating temperature by removing the high thermal resistance layers. Since the distribution is sharply peaked at the gate, the removal of just the PDMS layer closest to the gate would drive down the temperature considerably, as shown in Figure 7-12. Complete removal of PDMS would decrease the temperature another 10 °C, but would create some difficulty in bonding the Si modulator to the rest of the package [92-93].

The purpose of the top PDMS layer is for thermal insulation of the Si modulator and to serve as a dielectric between the GaN PA and the antenna ground plane. Since the operating temperature can be decreased by over 200 °C by removing this layer, alternatives were considered. By using a more conventional SiNₓ passivation, the dielectric qualities can be preserved, and the improvement in heat transfer is still considerable for thin films, as shown in Figure 7-13 [92-93].

The design of the device also plays an important role. Again a multiple finger design, can provide an improvement of ~40 °C over a single gate with 1 mm gate width with the proper gate pitch, as shown in Figure 7-14.

The effect of the boundary conditions was investigated, as shown in Table 7-1. It is assumed that a reasonable forced convection heat transfer coefficient was 30 W/m²·°C, whereas a free convection heat transfer coefficient would be 10 W/m²·°C. The fixed value boundary would correspond to the package being mounted on a chip carrier, which would function as another heat sink. The most realistic case would be a fixed temperature near 25 °C on the bottom and free convection at the top. Note that this improves the heat transfer considerably [92-93].
Table 7-1. Effect of boundary conditions on package temperatures

<table>
<thead>
<tr>
<th></th>
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<tr>
<td>Bottom</td>
<td>Forced</td>
<td>Free</td>
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<td>Fixed</td>
<td>Fixed</td>
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</tr>
<tr>
<td>GaN</td>
<td>124</td>
<td>227</td>
<td>141</td>
<td>57</td>
<td>57</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>96</td>
<td>198</td>
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<td>25</td>
<td>25</td>
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</tr>
<tr>
<td>Antenna</td>
<td>92</td>
<td>196</td>
<td>109</td>
<td>25</td>
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</tr>
</tbody>
</table>

Figure 7-1. First-generation prototype of integrated heat sink/antenna incorporating GaN PA and Si modulator

Figure 7-2. Concept of the 3-D multi-layer structure combining heat-sink antenna, GaN RF and silicon signal processing electronics
Figure 7-3. Example of heat transfer through a composite wall

Figure 7-4. Mesh used for finite element modeling.
Figure 7-5. Effect of substrate thermal conductivity on the junction temperature of the HEMT

Figure 7-6. Effect of silicon carbide substrate thickness on the junction temperature of the HEMT
Figure 7-7. Effect of power dissipation on the junction temperature of the HEMT

Figure 7-8. Effect of Si thickness on the junction temperature of the HEMT
Figure 7-9. Typical temperature distribution under base operating conditions in the GaN layer (top) and Si layer (bottom)
Figure 7-10. Typical temperature profile in a cross section of the structure zoomed in to the area near the gate.

Figure 7-11. Effect of HEMT power dissipation on the maximum temperature in both active layers.
Figure 7-12. Effect of the removal of top PDMS layer and both PDMS layers on the maximum temperature in both active layers at varying power levels

Figure 7-13. Effect of SiNx passivation thickness on the junction temperature of the HEMT
Figure 7-14. Effect of gate pitch on the junction temperature of the HEMT in a multiple finger configuration
CHAPTER 8
UV LASER PROCESSING

8.1 Overview

Excimer laser processing has emerged over the past 30 years as a powerful micromachining technique. They are particularly flexible tools due to their short wavelength, high efficiency, and high power. A sampling of the many processes that use excimer lasers are as follows: photoablation, etching, micron-scale lithography, doping, texurizing surfaces, planarizing and cleaning surfaces, and medical applications. The most notable development in the medical field is laser keratectomy with a 193 nm laser, known today most commonly as LASIK. It is also used in the electronics industry in several capacities, most notably being for via hole formation in dielectric films, but it is also used to selectively remove metal to rework circuits or masks where there are electrical shorts. Pulsed laser deposition is one of the most studied applications, and offers several advantages over conventional CVD or sputtering, the most notable being stoichiometric ablation of an alloy.

Pulsed long wavelength lasers such as the CO\textsubscript{2} and YAG lasers, were first developed commercially. They are used primarily for bulk micromachining, particularly engraving, of metal or ceramic parts. These lasers are quite limited though in that they are incapable of producing high-resolution features, reflection from the surface becomes more efficient at larger wavelengths, thus requiring more input power, and longer wavelength photons have less energy, so photochemical reactions cannot be initiated efficiently. For this reason the primary ablation is heating and subsequent sublimation, which can create damage in the material and debris on the surface [133].

UV laser processing is advantageous in that UV photons are capable of excitation of gas, liquid, or solid molecules, which is a first step in the photoablation process. UV photons are
strongly absorbed by most materials, so with decreasing wavelength, the range of materials that can be processed increases considerably to where nearly everything except quartz can be machined at 193 nm. UV light can also penetrate a laser induced plasma plume above the ablation site, allowing the etch to continue. Longer wavelength photons cannot penetrate this plume therefore the etch can be self-terminating as it reaches a point where the plume cannot dissipate before the next pulse occurs. UV lasers are also capable of producing high peak power, which is important for rapid processing and initiation of ablation processes, and high average power, which is important for a rapid, repeatable process (i.e. if each pulse has the same average energy, one can count the number of pulses for a precise etch depth control) [134].

Since there is no effective wet etchant for SiC, vias are currently formed using conventional dry etching techniques, such as Reactive Ion Etching (RIE) or Inductively Coupled Plasma (ICP) etching. The problem with these processes is that the typical etch rates in F₂- or Cl₂- based plasmas range from 0.2-1.3 μm/min. The typical substrate thickness is on the order of hundreds of micrometers and, even for thinned substrates of 50 μm, etching can take up to four hours under ion energy condition where mask erosion is minimal. Another disadvantage of the dry etching process is that the mask material must be robust, typically metals such as Ni, Al, or Cr. The deposition, patterning, and removal of the mask add complexity to the process, making it difficult for mass fabrication. There are also sidewall roughening and micromasking issues with dry etching, making the process very inconsistent [135].

Laser drilling appears to show promise for fabrication of via holes in SiC substrates. This is a maskless process, so there is no additional processing required beyond the actual drilling. The drilling is computer controlled, and the laser is focused only on the area where the hole is desired, so there are no loading effects observed, allowing for very reproducible results. With the
computer controlling, there is no physical mask to be made, which adds considerable flexibility and tuneability to the process. The etch rates are considerably higher (2-14 μm/sec) than dry etching, but this is a serial process. With the high etch rates, however, a single hole can be drilled within ten seconds with no additional processing required, making this process still faster than dry etching. The biggest issue that must be addressed is surface debris and the reliability of HEMT devices fabricated on laser drilled substrates [135].

Debris formation is in fact the motivation behind such an extensive study of drilling systems before purchase. The most ideal situation would be purely gaseous ablation products, which can easily be removed by a nozzle near the ablation point attached to a vacuum pump. In a real situation, the ablated material is “redeposited” on the surface of the sample and nearby mechanical components. Much like in a plasma etch, there will be volatile products, which will be easily removed, and nonvolatile products, which will remain on the surface. XPS can be used to identify the components remaining on the surface, and once known, methods of protecting the surface can be determined. As an example, an XPS study of polyimide ablation shows a carbon rich surface, implying that oxygen and nitrogen formed volatile products, most likely NOx and COx species, while the carbon was left as soot, which can be difficult to remove [136].

One interesting method of protecting the surface is by preventing the formation of such debris. A proposed method for this is to perform the ablation in either a vacuum or a chamber with a light gas atmosphere such as He, or flowing He over the sample. The reason for this is that the light atoms or vacuum will decrease the probability that the debris atoms will form clusters and increases the likelihood that they will stay in the gas phase and be swept away [136].

Typically a cleaning step must be performed after ablation. The exact nature of the clean will depend on the material and the nature of the debris formed. One possible method involves
using the laser again at a low energy to ablate the debris. This usually just results in moving the debris around on the surface to a safer location. For organic contaminants, an oxygen plasma can be used to ash the debris. Other chemical methods are also used, such as a rinse with acetone, an acid etch, or either combined with ultrasonic agitation. Finally, one of the more promising general use methods would be to coat the material with a sacrificial layer, such as photoresist, prior to ablation. This operates under the same principle as coating a sample with photoresist prior to dicing. The resist can be removed after ablation to leave the clean surface [136].

8.2 Solid State Laser Processing

Initial efforts to study via hole formation used industrial standard marking systems, which use solid state lasers. These systems are typically excellent for laser scribing of identification numbers, cutting, or welding of metal parts. It was ultimately determined that while these lasers are excellent for metal processing, the wavelengths do not couple well with semiconductors, ceramics, or polymers. This is due primarily to the increased reflection at these longer wavelengths relative to UV lasers (discussed in a later section). This implies that more laser power will be required to ablate material, which in turn will cause more sample heating. Metals, having a high thermal conductivity, can dissipate the heat more efficiently [133].

8.2.1 Background: Diode Pumped Solid State Lasers

Diode-pumped solid state (DPSS) lasers operate by using a laser diode to pump a crystal medium for gain. The crystal is typically neodymium-doped either yttrium aluminum garnet (Nd:Y₃Al₅O₁₂), better known as Nd:YAG, or yttrium orthovanadate (Nd:YVO₄). The neodymium replaces yttrium in the crystal lattice and emits at 1064 nm. While there are two types of crystals used, both are referred to as YAG lasers. Such lasers are capable of extremely high power by operating in Q-switched mode, which places an optical switch in the laser cavity
that is timed to open when the maximum population inversion is achieved. This maximizes the efficiency of the laser at its emitting wavelength [137].

With a 1064 nm base IR laser system, a series of nonlinear optics crystals can be used to generate higher order harmonics to alter the wavelength of the system. For example, lithium triborate (LiB₃O₅, LBO) can be used to generate the second harmonic frequency in the visible range of the spectrum at 532 nm. This is the method commonly used to create green laser pointers. A typical third harmonic generator is potassium dihydrogen phosphate (KH₂PO₄, KDP). This is used to generate the “frequency tripled” harmonic at 355 nm, creating now a UV laser. A “frequency quadrupled” laser can also be formed, emitting at 266 nm. While these capabilities come a cost. While a UV DPSS laser may be desirable, the price paid is power output. Typically the second harmonic generation is only 20% efficient relative to the YAG emission, thus the power level of a frequency doubled system is only 20% of a 1064 nm YAG system for the same laser. High harmonics will be less efficient, so one can imagine that for a UV DPSS system, one must start at a high output power laser to obtain any reasonable power output level [137].

The source is an optical beam, so the pattern shape is always circular, with the minimum feature size determined by the beam size, which is typically no smaller than 10 μm and can be up to 30 or 50 μm. Patterning is then achieved by trepanning, which is the process of translating the beam in the shape of the desired pattern to remove material. DPSS systems do offer advantages though in that they require no maintenance of the laser itself, so the only periodic maintenance cost will be upkeep on the optics. Since the DPSS laser is pumped by a solid-state source rather than a gas discharge, the pulse frequency can be very high (over 100 kHz). The low power output is compensated by this, so high etch rates can be achieved, and these systems are used for high throughput/low maintenance applications [138].
8.2.2 Experiments: Frequency Effects

The early work on this project built on the postdoctoral work of Dr. Suku Kim at UF, who explored via hole formation in SiC using laser processing [135]. The primary goal of this work has been proof-of-concept for the via hole process and to evaluate systems available on the market with the goal of purchasing one that will serve the purposes of research at UF. To that end, samples were sent to several companies for simple processing on their system to evaluate compatibility and limits. The primary methods used to quantify performance were feature size and the degree of damage and surface debris, both determined using a combination of optical microscopy and SEM.

The first studies evaluated the performance of systems at Lenox Laser and US Laser Corporation. These were selected as they were highly reputable marking systems, however they were typically used for metal processing. They both used a 1064 nm YAG laser, and US Laser provided the capabilities to study both frequency doubled and frequency tripled modes. This allowed us to effectively study the effects of decreasing the wavelength. Performance improved significantly when the UV region was reached, as predicted by the literature and mentioned in the discussion both above and below. In this set of experiments, a HEMT structure was used, and devices were fabricated on the sample after laser drilling [71, 74].

An AlGaN/GaN HEMT structure was grown by MOCVD on a SiC substrate (4H-polytype, N-doped, $\sim 10^{17} \text{cm}^{-3}$, thickness was $\sim 400 \mu\text{m}$). Laser drilling was employed in both directions, i.e. from front-to-back and vice versa. Via holes with nominal diameters of 50–500 $\mu\text{m}$ were obtained by laser drilling with a Nd:YVO$_4$ laser ($\lambda = 1064 \text{ nm}$), frequency doubled Nd:YVO$_4$ laser (532nm) or frequency tripled Nd:YVO$_4$ laser (355nm). The pulse frequency was up to 60 kHz at an average power of 11 W, leading to an average pulse energy of 183 $\mu\text{J}$. Mesas were
formed in the epi layer by ICP etching in a Cl2/Ar plasma (10 sccm/5 sccm) for 1 minute at 150 W ICP power with a chamber pressure of 2 mtorr. Ti/Al/Pt/Au contacts 100 µm square were deposited by e-beam evaporation and patterned by lift-off. These were annealed at 900°C for 1 minute under flowing N2. The anisotropy and surface morphology of the resulting holes were examined by SEM [71, 74].

Typical average ablation rates of up to 50 µm/sec were achieved, depending on the energy density of the laser pulse. The sidewall roughness of the laser drilled holes was comparable or better than those achieved with plasma etching. The absence in the laser drilled features of vertical striations, resulting from transfer of mask sidewall roughness during conventional plasma etching, is clearly an advantage of the former method. Since the laser drilling works by ablation of the SiC, there is also less of a problem with micromasking leading to so-called “grass” on the SiC surface as there is with plasma etching. However, the 1064 nm laser light source limits the feature size up to 40-50 µm. For the features less than 40 µm, it is difficult to control the dimension and shape. We found that the use of a 355 nm laser not only can reduce the dimensions of the drilled features, but also can improve the morphology of the drilled surfaces. As an example, Figure 8-1 shows SEM cross-sections of holes drilled at 1064 nm (left) and 532 nm (center). The latter produces an improved sidewall surface roughness, which is further improved at 355 nm (right). The SEMs in Figure 8-2 of holes drilled from the front of the wafer at 1064 nm (above) and 532 nm (below) show improved roundness and cleaner holes at 532 nm with similar amounts of surface redeposition in the two cases [71, 74].

Figure 8-3 shows a SEM image of holes drilled in the HEMT/SiC substrates at 532 nm from the front (above, left) and back (below, left) of the wafer and also at 355 nm from the front (above, right) and back (below, right); minor top-side surface damage is visible on holes drilled
from the front, while some epitaxial layer cracking is visible on holes drilled from the back-side. This is an indication of high thermally-induced stresses in the latter case and is clearly not acceptable for device fabrication [71, 74].

Figure 8-4 shows SEM at an angle of holes drilled from the front at 1064 nm (top), from the back at 355 nm (center), and from the front at 355 nm (bottom). The shorter wavelengths produce significantly cleaner and rounder holes, along with minimal surface damage.

The left picture in Figure 8-5 shows the undrilled alloyed Ti/Al/Pt/Au-based metallization in transmission line measurement (TLM) patterns. The dimension of the square metal pads is 100 x 100 µm². The center picture shows the same pattern on a substrate drilled with the 1064 nm laser. In this case, there is significant debris caused by the drilling, contaminating the areas surrounding the vias. The picture on the right shows a hole drilled with a 355 nm laser in the TLM region, without damaging the TLM pattern. Table 8-1 shows the electrical data from the TLM patterns before and after the laser drilling at two different wavelengths. The sheet and contact resistance from a 355 nm laser drilled sample are very similar to the undrilled reference sample [71, 74].

8.3 Excimer Laser Processing

Since the UV solid state laser performed much better than the IR solid state laser, it makes sense to try an even shorter wavelength using an excimer laser. A brief background section on excimer laser processing will be presented next, followed by results from a comparison of excimer and solid state laser drilled holes.

8.3.1 Background: Excimer Lasers

An excimer laser is a gas-phase system that uses electronically excited molecules to emit high intensity pulses of UV light. The term was originally meant as a shorthand for excited dimmer, which implies two identical atoms. Most excimer gases are actually heteronuclear
diatomics, thus the proper term, though not widely used, would be exciplex. A table of excimer molecules and their wavelength is listed in Table 8-2. Typically excimer lasers use a mixture of <1% halogen (F₂, Cl₂) gas, 2-5% rare gas (Xe, Kr, Ar), and the remaining 94-95% a buffer gas (Ne, He). The bulk of this discussion will refer to an ArF excimer gas at 193 nm. The primary reason for this is because this is the wavelength of the system that will be purchased, and therefore it is the most relevant wavelength. Note though that since an excimer laser is a gaseous source, the source gas and thus wavelength of the system can be changed by simply purging and filling the chamber with a different mixture. The optics must also be changed to be compatible with the new wavelength as well, but the entire assembly can be purchased for ~$5K [138].

The principle of operation is very complex. The buffer gas absorbs most of the initial excitation energy, then an electron is transferred to the halogen, creating a negative ion that bond rapidly with the rare-gas positive ion to produce an ion pair in an excited state. As the molecule falls back to a dissociated ground state, it emits at a characteristic wavelength (bound-free transition) [136]:

\[ \text{Kr}^+ + \text{F}^- + \text{Kr} \rightarrow \text{Kr}^+\text{F}^- + \text{Kr} \rightarrow \text{Kr} + \text{F} + \text{Kr} + h\nu \text{ (248 nm)} \]

The gain in this system is inherently high (up to 2x10⁴ in a single pass) since the density of excited states exceeds the unbound ground state population in the laser cavity. Excimer systems therefore do not require the high reflectivity cavity mirrors to provide optical feedback and can operate with a rear reflector and an uncoated front window. Excimer lasers are pumped by a fast electrical discharge. In this type of situation, the excimer action must be achieved before breakdown and arcing occur, so pulses are short (10-50 ns) [136].

All systems will degrade with time as the halogen gas slowly reacts and absorbing impurities form in the gas mixture. For this reason, a periodic maintenance issue with excimer
lasers is gas changing. The performance can be restored by purging the laser cavity and adding fresh gas. Gas lifetime is usually stated in terms of the number of pulses before the output power drops to half of the “fresh gas” output power. This depends on the wavelength (shorter wavelengths have shorter lifetimes) and laser design, but a typical range is $10^7$-$10^{10}$ pulses. For a system that is regularly used, this amounts to a gas change every ~2-3 months [138].

The beam size depends on the geometry of the discharge electrodes in the chamber, but typically ranges from 5-10 mm x 10-30 mm with a gaussian power profile along the short axis and a fairly level power output along the long axis. Because it is an optical beam, this can be focused and scanned serially, or exposed through a mask for parallel patterning. This is a particular advantage of excimer lasers over solid-state lasers, which are a point source. Excimer lasers are, in fact, advantageous over all other UV light sources because they operate by direct transitions between excited and ground states, as opposed to DPSS lasers, which operate on principle of generating harmonics to triple or quadruple the frequency and are inherently inefficient. They are also advantageous over UV lamps as they emit directed power rather than requiring collectors and reflectors. It is for this reason that excimer lasers are considered promising for deep-UV lithography applications [136].

Given the size of the beam, it is typically desirable to use some pattern generation process for image formation. There are several options for doing this. The first method is trepanning, which was described in the DPSS processing section. This is typically not used in excimer processing because the option is available to use masks. The masks are usually molybdenum plates with patterns formed in them reflecting the geometry of the image. For finer features, one can even use chrome on quartz lithography masks as well. As one can see, it is possible to pattern very complex features in a semi-parallel fashion with an excimer laser. The pattern can
then be stepped across a sample (i.e. a 4 x 4 array of squares can be stepped twice in each
direction to create an 8 x 8 array). The third, and most intriguing, method is to coordinate beam
scanning with stage translations to control the vertical dimension as a function of x and y
position. This can create stepped, sloped, or rounded walls [138].

The ultimate resolution of the beam will be determined by geometry, depth, optics, and
material properties. Patterning features to micron scale resolution is quite possible with
appropriate quality focusing optics, and 10 μm is possible with a standard system. There will be
an aspect ratio limitation as well though, with limitations from about 10:1 to 20:1, depending on
the material. Hard materials such as SiC will require a large fluence, and there will be a
demagnification factor associated with the projection process to achieve said fluence. This will
thus limit the feature size and aspect ratio achievable. For polymers and thin films, it is much
easier to achieve high resolution patterns because the material couples with the laser very well
[138].

Upon irradiation with a UV laser beam, four processes can occur: photolysis, electron
ejection/ionization, electron-hole pair generation, and heating. Photolysis refers to molecular
bond breaking, i.e. the following reaction:

\[ \text{AB} + hv \rightarrow \text{A} + \text{B} \]

The bond that is broken in the process can represent a bond between diatomic molecules,
resulting in individual atoms A and B; a bond within a molecule, creating fragments; a bond
between a molecule and a surface, resulting in desorption; or a bond within a molecular solid,
which is broken. This is the mechanism for laser ablation. This process occurs when the photon
energy from the laser beam excites a molecular bond, as typically the case with UV wavelength
lasers, and is the most relevant reaction for the purposes of this work. A schematic of the photoablation process is shown in Figure 8-6 [136].

If the photon energy (6.7 eV for ArF) exceeds the work function (3-5 eV) of a metal surface, a photoelectron will be ejected. This is relevant particularly with metal surfaces, and the ejected electron can actually serve to enhance a chemical etch by assisting in desorption of reaction products. Electron-hole pair generation occurs in semiconductors when the photon energy exceeds the bandgap of the material. The effects can be the same as photoelectron emission in metals, but it can also have potentially implications for reliability testing as the additional electron-hole pairs on a biased device will cause a higher current level and more stress on the device [136].

Sample heating is also a relevant process, and occurs when photon energy is converted into excited electronic states, which decay into ground state atomic vibrations, thus raising the temperature. Each pulse is able to raise the temperature very rapidly (up to $10^{10}$ K/s) because a large amount of energy is imparted into a small volume in a short time. This is complementary to the ablation process as it forces the sublimation or desorption of nonvolatile ablation products. At UV wavelengths, most of the photon energy goes into exciting molecular bonds rather than pure heating. The temperature can get very high on a per pulse basis (AC temperature rise), but the repetition rate is relatively low that the sample always reaches equilibrium temperature between pulses (DC temperature rise). For high pulse rates or long wavelengths, such as in a DPSS laser, the AC temperature may never reach the ambient value, leading to a rise in the DC temperature of the sample. This can cause damage to the material [136].

A distinction must be made between ablation and etching. In the context of laser processing, ablation refers to material removal purely by the interaction of the laser beam with
the material, while etching refers to the laser excitation of a chemical etchant for enhancement of the etch. To this end, pure laser ablation has been studied to date in this work. Laser etching could possibly be studied to selectively etch material, such as enhanced etching of GaN using KOH [136].

Ablation can be broken down into 3 areas: highly absorbing materials, weakly absorbing materials, and organics. Highly absorbing materials are capable of being intensely heated by the laser pulse. Ablation then occurs primarily by sublimation. Metals fall into this category, and it is for this reason that metals typically machine poorly in UV systems. There is usually an area around the periphery of the pattern where there is beam-induced damage in the form of an area that was melted during ablation. Another concern is thermal conductivity. Metals prove difficult to machine because, though they are highly absorbing, they tend to conduct the energy away very rapidly, thus requiring high fluence lasers to continuously provide sufficient energy on target. This is epitomized in an example of a Cu film. Bulk Cu is very difficult to machine with a UV laser and requires several J/cm² for ablation to occur, however ablation will occur at 0.1 J/cm² in a 1000 Å Cu film on an insulator such as SiO₂. This is because the low thermal conductivity of the dielectric confines the laser energy to the Cu layer [136, 138].

In weak absorbers, such as semiconductors, several processes may occur. First, basic photoablation can occur if the energy is larger than the bandgap, which will always be the case for an ArF laser. Second, multiphoton absorption can lead to electron generation and ionization, which will cause an avalanche breakdown process and generation of a plasma condition, resulting in material ejection. This is typically the case for insulators, which have a bandgap larger than the photon energy. Third, defects will play a major role by acting as localized absorption centers, which can cause heating, and subsequent breakdown and ejection. Ablation
of organics is typically photochemical, as organic bonds absorb strongly in the UV region. Polymers are usually a low thermal conductivity material, so there is heating occurring, but the primary ablation mechanism of photochemical [136].

8.3.2 Experiments: Laser Type

After settling on the UV laser as the ideal candidate for our system, we sought out a company with expertise in this area. It was here that we began working with Jeff P. Sercel Associates (JPSA Laser). They were able to machine samples using a DPSS 355 nm system and a 193 nm ArF system. As an initial test, samples of the SopSiC HEMT material from Picogiga (see Ch. 4) were sent to them. While there is a wavelength variation between the two systems, the primary comparison is between the DPSS and excimer laser performance. The wavelength effects are not as pronounced within the UV region as they are between visible and UV. Devices were not fabricated on these samples, so electrical measurements cannot be compared.

Samples were processed from the top surface down to the bottom surface. For the DPSS laser, the wavelength was 355 nm, with a pulse rate of 100 kHz and laser power of 1W. The excimer laser was an ArF laser at 193 nm, with a power of 5W and pulse rate of 1 kHz. Optical images are shown in Figure 8-7, and SEM images in Figure 8-8, with DPSS on the left and ArF excimer on the right. It is clear even from the optical images that there are burn marks on the surface of the DPSS laser sample. In addition, self-terminating effects discussed previously were witnessed with the DPSS laser due to the high pulse rate and high aspect ratio. This placed a severe limit on the feature size for thick samples, with an aspect ratio of about 5:1. Given that the sample can be up to 500 μm thick, a minimum feature of over 100 μm is not acceptable. The excimer laser was able to form features down to 30 μm in diameter in the same sample. In
addition, there is less surface debris on the surface of the sample processed with the excimer laser, where it is just a small radius of material.

To further examine the drilling processes, the samples were cross-sectioned with a dicing saw. The SEM images are shown in Figure 8-9, with the DPSS hole on the left and excimer on the right, and low magnification on the top and high magnification on the bottom. The excimer hole shows some taper towards the bottom of the hole. This is characteristic of excimer laser processing, and is actually beneficial for the purpose of the via hole process because the tapered hole will facilitate metallization. The degree of taper can be controlled with the laser parameters, and if perfectly straight holes are necessary, either a higher power or overablation can be used. The disadvantage of higher power is that some control over the etch rate is lost. The excimer holes show a smoother surface with less beam-induced damage. There are obvious molten regions on the DPSS hole, visible at high magnification.

As another test, an array of holes in InP and GaAs was formed. The optical image is shown below in Figure 8-10. An 8x8 array of holes were drilled through a 150 μm thick wafer with an entrance hole diameter of 110 μm and exit hole diameter of 100 μm, with a pitch of 200 μm. While these were processed serially, it would be possible to create a mask that could be stepped, such as the one described above (a 4 x 4 array stepped twice in both the x and y direction). This test showed very good feature control and reproducibility.

Ultimately it was decided that the JPSA IX-260 machining system was perfect for the needs of the research group and the university. It offers the resolution and flexibility of materials that are necessary. It will be configured initially for 193 nm, but can be altered to perform at any excimer gas wavelength. In addition, high-resolution optics are available to achieve micron-level resolution. It has been fitted with an air-bearing stage that provides 0.1 μm resolution and 1 μm
repeatability over the entire 6-inch range of movement. A system has been ordered and will be
installed in spring 2008.
Table 8-1. Electrical data demonstrating the effect of laser drilling on etching and contact properties

<table>
<thead>
<tr>
<th>Process</th>
<th>Drill Direction</th>
<th>Rs (Ω/sq)</th>
<th>Rc (Ω-cm²)</th>
<th>Mesa Depth (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference</td>
<td>No drill</td>
<td>368 ± 23</td>
<td>2.97 x 10⁻⁵</td>
<td>950</td>
</tr>
<tr>
<td>1064 nm drilled</td>
<td>Back to front</td>
<td>644</td>
<td>5.74 x10⁻⁶</td>
<td>350</td>
</tr>
<tr>
<td>1064 nm drilled</td>
<td>Front to back</td>
<td>421</td>
<td>1.53 x10⁻⁵</td>
<td>0</td>
</tr>
<tr>
<td>355 nm drilled</td>
<td>Back to front</td>
<td>361 ± 44</td>
<td>6.33 x 10⁻⁵</td>
<td>945</td>
</tr>
<tr>
<td>355 nm drilled</td>
<td>Front to back</td>
<td>362 ± 22</td>
<td>2.83 x 10⁻⁵</td>
<td>945</td>
</tr>
</tbody>
</table>

Table 8-2. Excimer laser gases and wavelengths

<table>
<thead>
<tr>
<th>Wavelength (nm)</th>
<th>Emitting Molecule</th>
<th>Relative Pulse Energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>157</td>
<td>F₂</td>
<td>0.05</td>
</tr>
<tr>
<td>193</td>
<td>ArF</td>
<td>0.6</td>
</tr>
<tr>
<td>222</td>
<td>KrCl</td>
<td>0.1</td>
</tr>
<tr>
<td>248</td>
<td>KrF</td>
<td>1.0</td>
</tr>
<tr>
<td>308</td>
<td>XeCl</td>
<td>0.8</td>
</tr>
<tr>
<td>351</td>
<td>XeF</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Figure 8-1. SEM cross sections of holes drilled at 1064 nm (left) and 532 nm (center)
Figure 8-2. SEM images of hole drilled from front at 1064 nm (above) and 532 nm (below)
Figure 8-3. SEM image of holes drilled at 532 nm from front (above, left) and back (below, left) and 355 nm from front (above, right) and back (below, right)
Figure 8-4. SEM at an angle of holes drilled from the front at 1064 nm (top), from the back at 355 nm (center), and from front at 355 nm (bottom)
Figure 8-5. Photographs of TLM patterns with Ti/Al/Pt/Au based metallization on an undrilled sample (left), drilled with 1064 µm laser (center), drilled with 355 nm laser (right).

Figure 8-6. The UV photoablation process.
Figure 8-7. Optical microscope images of front and back of via holes formed in poly-SiC substrates with a DPSS laser (left) and excimer laser (right) from the top semiconductor surface (top) and bottom SiC surface (bottom).

Figure 8-8. SEM images of via holes formed in poly-SiC substrates with a DPSS laser (left) and excimer laser (right) from the top semiconductor surface.
Figure 8-9. SEM images of cross-sections of via holes formed in poly-SiC substrates using DPSS laser (left) and excimer laser (right) at low magnification (top) and high magnification (bottom)

Figure 8-10. Optical image of array of holes formed in GaAs
CHAPTER 9
ELECTROLESS METAL DEPOSITION

9.1 Overview

While the electroless metal deposition project was initially studied for metallization of via holes in SiC, the most interesting device application that has emerged has been its use for hard mask deposition for dry etching. To this end, the following section will provide an overview of the fundamentals of Ni deposition, followed by an overview of a photovoltaic device that has been fabricated in SiC using electroless Ni as an etch mask.

9.1.1 Nickel Plating

Electroless (or catalytic) metal deposition is a subset of the general category of nonelectrolytic metal coating processes. All metal depositions from solution follow the same general mechanism, in which the metal in solution is reduced by a source of electrons to the solid state on the surface to be coated, shown in the following reaction:

\[ M^{x+} \text{(aq)} + xe^- \rightarrow M \text{(s)} \]

In a typical electrodeposition process, this reaction is quite straightforward, with the electrons being supplied by an external power supply. In this case oxidation occurs at the anode, producing the metal ions from a solid source into solution, and at the cathode the ions are deposited onto the surface of interest by the reduction reaction given above. An electroless plating method follows this same principle, but the reactions occur simultaneously in solution with no external source required. This process is, therefore, considerably more complex and not completely understood as of yet [139].

Nickel is a metal of interest both for via hole filling and as an etch mask for SiC during dry etching. Since the etch rates are so slow, the mask material must be quite robust, since it will be sputtered away during the etching process. This calls for a very thick mask, approximately 10
μm. This cannot be deposited using standard microelectronic fabrication methods such as evaporation or sputtering, but it can be accomplished using electroless deposition. [139]

The procedure for electroless deposition is straightforward. First, a nonmetallic substrate is cleaned and etched. The substrate is then activated and sensitized in a tin and palladium process, which is the catalytic activator for the electroless bath. The Pd surface initiates the deposition reaction. At this point, the process becomes autocatalytic, and small islands form around the adsorbed Sn/Pd sites, spreading laterally until they meet, forming a continuous conductive surface. Electroless nickel has actually been proposed as an alternative to copper, offering the advantage of better stability and process development [139].

The electroless nickel process was developed industrially in the 1950s. It is widely used in industry as a coating process due to the wear and corrosion resistance of Ni. The standard reducing agent for Ni is sodium hypophosphite (NaH2PO2). If the Ni salt and sodium hypophosphite are allowed to react, the Ni is precipitated as a sludge, which is of little use. An organic acid is typically added as a complexing agent and buffer. It was first shown by Scholder and Heckel in 1931 that the product formed in this reaction is actually a Ni-P alloy, with the phosphorous inclusion coming from the decomposition and incorporation of the hypophosphite ion in solution. One mechanism for the reaction is shown in the following reactions:

\[
\begin{align*}
H_2PO_2^- + H_2O &\rightarrow HPO_3^{2-} + 2H^+ + H^- \text{ (acid solution)} \\
H_2PO_2^- + 2OH^- &\rightarrow HPO_3^{2-} + H_2O + H^- \text{ (alkaline solutions)} \\
Ni^{2+} + 2H^- &\rightarrow Ni + H_2
\end{align*}
\]

This mechanism explains the observed simultaneous reduction of nickel and evolution of hydrogen gas. Many other mechanisms have been proposed, including simultaneous catalytic and electrochemical processes. This is a testament to the complicated nature of the process [139].
Acid solutions present many benefits, including higher deposition rates, greater stability, and improved physical characteristics of the deposition. The general reaction is as follows:

\[ \text{Ni}^{2+} + \text{NaH}_2\text{PO}_2 + \text{buffers, complexors, stabilizers} \rightarrow (\text{Ni} + \text{P}) + \text{H}_2 + \text{NaHPO}_3 \]

This reaction takes place on a catalytic surface, either activated using Sn/Pd or an acid-activated seed metal surface. Iron has been discussed as a seed metal, but it is a deep level trap for most semiconductors, making it of little use. Also discussed have been Pt and Ni. The most common salts used for the Ni source are the chloride and sulfate, in concentrations of 4-10 g/L. Sodium hypophosphite is virtually the only reducing agent for Ni. The reduction potential for Ni is \(-0.2 \, \text{V}\), so this reaction requires a strong reducing agent. The buffers and complexors are typically single ingredients, and almost all are organic acids. These stabilize the pH of the bath and mildly complex the Ni. Again, moderators and wetting agents can be added if necessary.

Temperature is the most important factor that influences deposition rate, with essentially no deposition occurring below 50 °C, and most baths operating between 80 and 100 °C [139].

### Alpha-Voltaics

An alpha-voltaic device is very similar to a solar cell, except it operates by producing power from alpha-particle radiation rather than solar (visible) radiation. This is particularly useful for portable power supply applications, in which a radiation source is coupled to the devices, thus producing a completely self-contained long-lifetime power supply. Alpha-voltaics are particularly attractive over beta-voltaics due to the less strict shielding requirements for alpha particles. The device consists of an alpha radiation source coupled with a semiconductor p-n junction, which will collect the electron-hole pairs created by the particle as it penetrates the material. The limiting factor in the development of these devices has been the radiation damage to the semiconductor. While the radiation source is stable over a long time period (Americium-
241 is typically used, which has a half-life of 432.7 years), the semiconductor is damaged within a matter of hours, thus reducing the power output. To this end, SiC is particularly attractive due to it’s inherent resistance to radiation damage. A schematic of such a device is shown in Figure 9-1 [140].

9.2 Electroless Plating Procedures

Initial testing used a basic solution formulated in the lab. It operates on the principle of the reactions described above. Most industrial solutions are based on this on a fundamental level, with many proprietary chemicals added to improve stability and to tailor the solution to specific applications (i.e. high rate, selective deposition, etc). While this is useful in determining the fundamentals of the process, it is impractical for real processing because the solution will be inherently unstable. Therefore when investigating a plating process for a real application, such as the MIPS device described above, commercial solutions were used. Results and observations from both are described.

9.2.1 Solutions Made In-House

Electroless Ni deposition on Si has been demonstrated using the following bath conditions: NiSO₄ (29 g/L), NaH₂PO₂ (17 g/L), sodium succinate (15 g/L), and succinic acid (3.2 g/L). A 500 mL solution was made of these components, as well as 200 mL solutions of the following two pretreatment solutions: SnCl₂-HCl (0.1 g/L-0.1 mL/L) and PdCl₂-HCl (0.1 g/L-0.1 mL/L). Initially, various preparation methods were used to determine the best method of initiating the reaction. If the aqueous Pd pretreatment is used, then, of course, Pd will adsorb on all surfaces contacting the solutions, causing Ni to plate everywhere. Since we are searching for a patternable plating process, this is clearly undesirable. Evaporated Au, Ni, and Pt (1000 Å) were also investigated, and it was found that only Ni functioned as a catalytic surface to initiate the reaction. Using sputtered Ni as a seed metal, followed by activation in the pretreatment solutions
for 2 minutes each, with rinsing between, then plating at ~60 °C and a pH of 5.8, a deposition rate of approximately 2 μm/h has been demonstrated [141-143].

Initial efforts resulted in delamination of the film. This was first thought to be caused by stress due to the high plating rate. The delamination phenomenon was still observed even when no plating was taking place. Annealing could help with adhesion, but there was still film peeling around the edges. The plating bath is slightly acidic, so when plating for hours, it will slowly attack the native oxide on Si. This will undercut the metal, resulting in delamination. Surface preparation is, therefore, essential. The oxide must be removed from the substrates by etching in BOE in the case of Si. To ensure there is no oxide on the surface between cleaning and deposition, a cleaning step was used in the sputtering system. This step biases the sample chuck, causing the ions to essentially sputter the chuck instead of the metal. This will remove all oxide and result in the best adhesion. The next issue is oxide formation on the metal surface. It has been observed by testing the selectivity to bare Si vs SiO2 that even activated SiO2 will not plate. The same trend appears to follow for most metal oxides. Before plating, the metal surface must be cleaned to remove the oxide. Several methods have been investigated to protect the Ni seed metal surface. The first method is simply by etching the NiO in NH₄OH, which is selective to NiO over Ni. The procedures and times for this process have not been investigated in detail. The method currently used involves sputtering a thin layer of Ti on top of Ni. This will protect the surface until plating. The Ti and TiO₂ that form can both be etched in BOE, and then rinsed and put straight in the plating bath without being dried, which would expose it to potential oxidation [144].

The next step is to make the process patternable. If a seed metal is activated and then selectively removed in a lift off process, the pretreatment will follow on those areas, leaving
activated seed metal areas, which will plate at a rate varying with temperature, and the nonactivated substrate, which will not plate. Work is in progress to optimize this process. Preliminary results show that an increase in plating rate and decrease in plating selectivity is observed by increasing the temperature to ~90 °C; therefore, the most optimal temperature appears to be ~70-80 °C. Studies of the pretreatment process show that different seed layers require different pretreatment processes. It appears that the SnCl₂ process may actually have a negative impact on the Ni process with seed metal, with improved uniformity, rate, and initiation, all at lower temperatures being observed with simply a 30 second PdCl₂-HCl pretreatment. The pretreatment step is critical, since if the sample is pretreated too long, there will be bridging of the features. The plating rate is highly temperature dependent, with observed rates of ~2 μm/h at 60 °C and ~7 μm/h at 75 °C. This process has been used to form a pattern consisting of a uniform layer of Ni with holes patterned that could be etched, as shown in Figure 9-2. The films were deposited at varying temperatures and, therefore, have varying thickness [144].

The plating bath as formulated is highly unstable. The deposition rate is temperature dependent and pH dependent, which are conditions for potential runaway reactions. Note that in the reactions presented above in acid solution, 2 H⁺ ions are evolved and only one H⁻ ion. Therefore the pH of the solution will decrease as the reaction proceeds. The reaction is buffered by the organic acid, but if the buffering capacity is exceeded, the pH can rapidly decrease, accompanied by a temperature increase, culminating in a runaway reaction where the all of the nickel precipitates as a sludge, accompanied by significant evolution of hydrogen. This entire process can occur in less than one minute. The reaction can be stopped by making the solution neutral again through the addition of NaOH [144].
The next step is to repeat these results on SiC. The transition proved quite difficult. Initial efforts to duplicate the process were failures in that the metal film always delaminated. Ultimately, it was determined that surface conditions are absolutely critical to the process. The SiC samples from one company resulted in delamination after less than one minute in the plating bath, while samples from a different company, which will have a different surface condition, will plate easily. It was determined that the “homemade” solution is too unstable for a reproducible process. Commercial plating solutions are readily available and testing has produced stable and reproducible results requiring considerably less solution and effort.

9.2.2 Commercial Plating Solutions

The first commercial plating solution investigated is known by the trade name Nickel-B from Transene. This solution was chosen because it resembled the solution produced in the lab in that it requires an activator (therefore is selective) and grows Ni films at a very high rate (desirable to reduce process time). A water bath in a double beaker system was used to maintain a constant temperature of 64-66 °C, and a 31:1 solution of activator to Nickel-B was used. A growth rate of 0.2 μm/min was observed. This film actually grew too fast and resulted in a very strained film, which peeled off after about 1 μm was grown.

Based on the observations from the Nickel-B experiments, it was determined that many of the problems were due to the fast growth rate. A different solution, known as Nickelex, also from Transene, was recommended due to the slower growth rate. The primary disadvantage for this solution is that it is not selective and a seed layer is required, thus some work is necessary to make a pattern in the film. The seed layer was e-beam evaporated Ti/Ni (200/800 Å). The Ti layer is meant to improve adhesion. Since the film requires a clean seed layer, the samples must be acid etched to remove any native oxide and create a clean Ni surface for plating. The etch
uses a 3:1 HNO₃:BOE solution for 10s. This will selectively remove NiO. The plating then proceeds at 65-70 °C using a double beaker water bath to control temperature, and the plating rate is 50 nm/min. A major drawback to using such long processing times is that bubbles form on the surface as H₂ gas is evolved as a reaction product. This results in localized pitting of the surface. The bubble effect can be reduced by directing solution over the surface using a pipette every 3-5 minutes, which is the same time scale as bubble formation. More advanced recirculators could be purchased for large-scale implementation. This process can be made patternable using the same method as electroplating operations – deposit a seed layer over the entire surface, then pattern the areas to be plated with photoresist. The areas opened with photoresist will then be plated up and the areas covered will not. This method is preferred to performing lift-off and then selectively plating because the former method results in a more uniform electric field on the surface and thus more uniform plating. The latter method provides no effective charge dissipation and thus each nickel pattern will have a different surface potential and thus plating rate. Other problems encountered was that, much like previous observations, the solution will deposit on any rough surface, hence a film will grow on the rough back side of Si test wafers and on any scratched surfaces in the plating beaker. All components must therefore be cleaned thoroughly in an aggressive aqua regia etch before plating [145].

The seed layer can be removed by plasma etching. Conveniently the plasma etch conditions used for SiC etching contain a sufficient physical component that the seed Ni can be easily etched away, while the plated Ni is sufficiently thick that it can withstand the etch to the desired depth. The plasma etch was performed in an ICP etch system using a SF₆/O₂ (25/2.5 sccm) plasma. The ICP power was 500 W and the RIE power was 200 W. The SiC etch rate was 200 nm/min [145].
For the MIPS project, this allowed for formation of 8 μm mesas in SiC (etching down to the n-type layer). The Ni can then be stripped very rapidly and selectively using an aqua regia etch (1:3 HNO₃:HCl). Further processing involves the deposition of the n-type ohmic contact, which is Ni, patterned by lift-off and annealed at 700 °C. The p-type ohmic contact is also deposited by evaporation, and consists of Al/Ti/Au, annealed at 200-300 °C. A passivation layer of 1000Å SiNx is deposited by PECVD. This represents the entire device structure, shown in cross section in Figure 9-4. An optical image of a 10 finger device is shown in Figure 9-5 [145].
Figure 9-1. An $\alpha$-voltaic battery
Figure 9-2. Optical microscope pictures of Ni plated on Si (4 μm on top, 11 μm on the bottom), with exposed holes
Figure 9-3. Photo (top) and optical microscope image (bottom) of Ni hard mask for SiC trench etching.
Figure 9-4. Cross-section of SiC MIPS device
Figure 9-5. Photo (top) and optical microscope image (bottom) of MIPS device fabricated using an electroless Ni etch mask.
10.1 Overview

Flip-chip bonding is one of the biggest advances in packaging technology. It has been used primarily as a method of packaging high performance electronic components to achieve shorter bond lengths, smaller chip size, and a higher I/O density. A new trend that is emerging is the use of flip-chip bonding for device integration, particularly for MCM electronic devices and MEMS devices. This process involves individually fabricating and optimizing components (i.e. an amplifier and a sensor) and then integrating them using flip-chip bonding. This can be viewed as a system-on-package (SOP) approach, rather than system-on-chip (SOC) approach, which involves directly fabricating all components on one chip. The disadvantage of the SOC approach is that process integration is particularly difficult, such as integration of Si and compound semiconductors on one chip, and typically performance of one or both components must be sacrificed in order to achieve the desired integration.

Standard flip-chip processing has been discussed in Chapter 3. This chapter focuses on the usage of flip-chip technology to integrate electronics components (in this case a VCSEL) and MEMS (a DBR structure) to create a hybrid device. The goal of this work is to create a tuneable filter. The DBR structure is a GaAs/AlGaAs superlattice and the emitter is a Si-based reflector to demonstrate the concept. The ultimate goal would be to fabricate a tuneable filter where the DBR structure is electrostatically actuated using metal arms. By raising and lowering the DBR, one could change the resonant frequency of the device, thus creating a tuneable filter. This approach is a very hot research topic and many such integration schemes have been proposed. Another such idea involves bonding a photodetector directly to an amplifier chip [146-148].
The device structure is shown in Figure 10-1. It consists of an Au reflector on a Si substrate, surrounded by poly-Si actuator arms bonded to a DBR structure, which is a GaAs/AlGaAs superlattice. The bond pads are 50 μm squares. The DBR structure is formed by an RIE etch, and there is a 5x6 array of devices on a die. After bonding, the substrate is removed from the DBR chip by etching a sacrificial AlAs layer in HF. The actuators are then released by another HF etch. Different HF concentrations are used to selectively etch each sacrificial layer [146-148].

10.2 Bonding Studies

Initial tests on this project involved finding a compatible materials system for bonding. While each component can be fabricated separately, a compatible bonding material that could be deposited in-house needed to be studied. Several candidates were proposed, including In, Au, and SU-8 polymer. The first efforts focused on metal bonds. In each case, bonding was performed at a matrix of conditions of temperature and pressure. For the metal bonds, large area die were used for bonding, then cross-sectioned and observed in the SEM. This was used to look at the amount of voids that formed and to look at the grain size. This is particularly important because the In film was rough as-deposited, so there is a considerable amount of voids formed at the interface. In another test, one side was totally removed, equivalent to the post-processing that would be experienced by the device chip, and surface scans were performed to study the roughness at the interface [146-148].

In the case of the polymer SU-8 bonding, different tests were performed. The polymer was chosen because the range of temperatures and the reliability was more compatible for the desired process, and polymer was used because only a mechanical bond was needed. In this case, the materials were bonded at a temperature and pressure matrix and the die were then pried apart.
Though systems are commercially available to shear die apart and measure the stress, none are available at UF. To that end, the “quality” of the bond was more a qualitative assessment as to at which temperature the bond was “hardest” to shear off. After the die were split, they were observed under the microscope to look for the deformation of the pad and any delamination. Based on these images, an optimized bonding program was built and devices were successfully bonded. All bonding tests were performed at UF, while the design and pre/post processing and testing were performed at AFRL [146-148].

10.2.1 Metal Bonding

Again, the first systems studied were In-Au and Au-Au pads. Since the actual device die were fabricated at a foundry at some time and cost, it is desirable to preserve this material as much as possible. Therefore, test die were fabricated from Si with either just the bond pads patterned or just a metal film deposited, and the DBR die were fabricated as they would be for the real device. After bonding, the package underwent the release processing, and the mesas were observed for cracking or complete breakage [146-148].

The first material set tested was Au-Au. This is the simplest system to fabricate. Experiments were performed to test the bonding over a pressure range of 1-1.5 kg and a temperature range of 300-400 °C. It was ultimately determined that the optimal pressure was 1.3 kg and temperature was 375 °C. While this was moderately successful in testing with dummy die, testing of real samples yielded either cracking or complete destruction of the die. This is because the high temperatures and relatively high pressures from the bonding process were not compatible with the MEMS process [146-148].

The next material set tested was In-Au. This yielded considerably better results in testing dummy die. A temperature range of 162-248 °C and pressure range of 200-400g were tested.
Cross-section SEM was used at first to study the quality of the bond formed. A typical result is shown in Figure 10-2. From the image, one can see that there is a significant quantity of voids in the In layer, and a large grain size (>2μm). The bond program was optimized as a stepped pressure profile. This will allow for the In to soften at a lower pressure (200 g) as the temperature is increased, then a higher pressure (400 g) is used to perform the controlled collapse above the melting point (200 °C), followed by cooling. The low bonding pressures can be achieve using In at the bonding metal because it is quite sticky, and it has a low melting point, making it an ideal candidate. In is usually deposited using lift-off of a thermally evaporated resist. Films are usually 5-10 μm thick, so a very thick resist is required for the process. Ultimately these films did not stand up mechanically to the release steps either. While the device remained intact due to the low temperature and pressure, the HF release step is not compatible with In [146-148].

10.2.2 Polymer Bonding

Since no electrical contact is required, polymers can be investigated. SU-8 has been demonstrated as having a low temperature and pressure bonding requirement, and is resistant to HF. As a test study, bond pads were deposited on Si, the pieces were bonded at a matrix of temperatures and pressures, 105-165 °C and 800-1200 g. After manual separation, both die were observed in an optical microscope, as shown in Figure 10-3. One can see that at the lowest temperature, the bond quality was poor as each set of pads adhered to the substrate, but were easily separated where they were bonded together. At the highest temperature, on the other hand, the pads bonded to each other, but deformed and began to shift. At the middle temperature, there is a solid bond formed, but minimal deformation. It was therefore determined that the optimal bonding profile is 135 °C, 1 kg pressure, for 10 minutes. This particular temperature was chosen
because it offered the lowest temperature to still make a solid bond that exceeded the strength of
the bond form the pad to the substrate. Real devices were then bonded using this method and
successfully released. An optical microscope image of the device die is shown on Figure 10-4,
and an image of a bonded die after release is shown in Figure 10-5 [146-148].

10.3 Device Demonstration

After device fabrication, the die were bonded to carriers and wire bonded for testing.
Reflectance was measured using a white light source directed at the reflector structure. A tuning
voltage range of 0-10V was investigated and a reference sample consisting of Au evaporated on
Si was used as a reference reflectance standard. The results are shown in Figure 10-6. A
wavelength tuning range of 930-990 nm was achieved. Though the design range matches the
actual wavelength range, the design actuation voltage vs wavelength curve does not correlate
well compared to the real measurement. The reason for this is mainly due to stress factors that
were not accounted for. The DBR was not planar, and actually formed a concave cavity. This
was verified using interferometry, with the data shown in Figure 10-7. When a simulation was
performed using a nonplanar cavity, the results correlated well with real device results, shown in
Figure 10-8. All design, simulation, and testing was performed at AFRL, while the bonding was
performed at UF [146-148].
Figure 10-1. A tuneable filter device

Figure 10-2. SEM cross-section of In film bonded to Au film
Figure 10-3. Optical microscope of test die after separation at 165 °C (top), 135 °C (middle), and 105 °C (bottom)

Figure 10-4. Optical microscope images of actual MUMPS die (left) and DBR die (right)
Figure 10-5. Optical image of a bonded device

Figure 10-6. Device testing results using a white light source compared to design simulations using a planar cavity
Figure 10-7. Interferometry data showing the curvature of the DBR

Figure 10-8. Device testing results using a white light source compared to calculations based on a curved cavity
CHAPTER 11
FUTURE WORK

11.1 Processing Studies

In pursuit of a functional prototype of the 3-D package concept described above, the goal for HEMT fabrication is to design and fabricate high power devices compatible with the laser drilling process. Work must be done to investigate fully the effect of laser drilling by examining HEMT performance before and after laser drilling. On the packaging level, work will also include investigation of novel oxide dielectrics for device passivation and packaging. To further push the state-of-the-art of AlGaN/GaN HEMT technology, e-beam lithography based “T-gate” or “mushroom gate” process needed to be used to achieve very small gate contact area, which improves the RF characteristics and, at the same time, have the large trace on top, minimizing gate resistance and further enhancing the RF performance.

11.2 Reliability

The topic of reliability is very critical for the realization of any practical uses of the nitride HEMT technology. Typical rf stress test systems can be quite expensive ($250K for 8 channels, up to $1M for >50 channels), so we are in the process of building one reliability test set at UF using a design adapted from Sandia National Labs. After completion of this system, there is a tremendous amount of interesting dc and rf reliability tests that can be done, as there is little work performed to date. Primarily, there should be an investigation into the failure mechanisms of AlGaN/GaN HEMTs, by stressing devices under a combination of DC, RF, and thermal stress. FIB and TEM analysis can be performed to look at the semiconductor layers. Typically, for the conventional III-V devices, failure rate can be linearly related to thermal stress, therefore accelerated testing is performed at elevated temperature. This is not the case for rf nitride based
HEMTs, therefore the ultimate goal of such a test system would be to derive an accelerated test program.[ref] Beyond this goal, the system will be of great use for any novel device structure.

At present, the temperature controller boxes are assembled and the final components for the RF driver boxes. DC power supplies for source-drain bias must be purchased, along with the required PCI boards for monitoring power output and supplying gate bias control. The programming must be performed in LabView to automate the system to control DC bias, RF power, and temperature, while monitoring DC current and RF power output.

### 11.3 Gas Sensors

A significant amount of work has been performed in our group on gas sensors. At present, the most marketable sensor is the wireless hydrogen sensor. The sensitivity range and response is competitive with other sensor technologies. One advantage of using GaN HEMT sensors is that the current change will be directly related to the gas concentration. Therefore work should be done to correlate the relationship and integrate into the programming in the data acquisition program. This would then allow the user to set a given threshold value in terms of a real parameter, rather than just hard coding a current change threshold that will not have much meaning to an end-user.

### 11.4 Simulations

The work to study heat transfer through the 3-D package has been wrapped up, but finite-element simulations will be important for all new devices at the packaging level. In particular, this type of simulation could be performed on hydrogen gas in a room to look at the gas flow pattern and better choose sensor installation sites, or even redesign the sensor package to incorporate a concentrator to better detect small leaks. It will also be beneficial to revisit thermal simulations after reliability studies have been performed. The reliability study will give a good
idea of the device response to thermal stress, which can be fed into a thermal simulation to
ing intelligently design a package to search for problem areas and remove heat as necessary.

11.5 Laser Drilling

Laser drilling has been studied thus far to evaluate systems for purchase and installation at
UF. The installation of a JPSA system will occur January 2008. This system will be a great asset
to the research group. Laser processing has been used primarily in industry, and to that end, there
has been little published, and little studied in depth. First of all, this piece of equipment can serve
as a versatile rapid patterning system. For rapid prototyping applications, there will be no need to
make a mask or go to a special job shop for micromachining applications. A wide range of
materials, from polymers to ceramics, semiconductors, and metals can be patterned to various
depths using this system. This opens up the possibilities for collaboration with new groups in
Mechanical Engineering, for example, who would have great interest in creating controlled
microstructures on a rigid surface.

A second area of major importance is the analysis. Again, since this has been an industrial
application, little research has been performed to study the laser machining process. While the
ablation mechanism can be studied through simulations and high speed photography, little true
materials analysis has been performed to study laser-induced damage in particular. The extensive
analysis equipment available at the Major Analytical Instrumentation Center at UF will allow
future group members to perform a full battery of tests on materials after laser ablation. In
particular, XPS and TEM will be useful, with TEM used to look at the thickness of a damaged
layer after laser processing and XPS used to probe the surface, to look at changes in the bond
structure after ablation. AES will also be a useful tool to study redeposition to determine the
nature of redeposited species and come up with methods of protecting the material from debris
contamination.
11.6 Electroless Plated Metal

While this phase of the project has been completed, this process will prove very useful for device applications. Dr. Brent Gila in Materials Science Department has used this process with a commercial plating solution to deposit films several microns thick with good uniformity and reproducibility. The device structure is particularly interesting in that the device uses SiC semiconductor, and Ni forms a good ohmic contact to this material. Therefore, the device structure uses the nickel film as an etch mask and then can be left on to form self-aligned ohmic contacts. Further work can be done to integrate this concept to device processing for niche applications.

11.7 Flip-Chip Bonding

Work has been completed on most flip-chip bonding projects at present. This is still an active area of research, and is particularly important for 3-D integration. There are two primary areas in which work can be done. First is the device level packaging process for RF HEMTs. Wire bondings introduce parasitic impedances due to the long transmission lines and curved nature of the bond wires. These have proven very difficult to model for the design of matching circuits. Flip-chip bonded devices should have a shorter transmission line distance in a straight line path. This should improve RF performance of packaged devices. The installation of the SolderJet system will allow for reliable in-house bumping of devices, so a direct comparison between devices processed at the same time from the same wafer should be possible.

The next area of interest is the physical design of the package to optimize performance and reliability. Flip-chip bonding can be used for photodetectors to allow for back-side illumination, which will enhance the efficiency. A particularly new area of study is component integration to create hybrid packages, similar to the 3-D project described in this work. The integration of CMOS, compound semiconductor devices, and MEMS is possible through flip-chip bonding,
such as the project studied in Chapter 10. Further work on this type of packaging level project is possible to create novel device structures.
CHAPTER 12
CONCLUSION

Wide bandgap semiconductor devices present interesting challenges to those of us involved in the field. The group III-nitrides are a particularly new class of compound semiconductors and show superior properties for high speed, high temperature, and high power applications. They will enable us to expand to areas we have never been with semiconductors before. GaN-based electronic devices are beginning to see commercial production in 2006, but there is still work to be done to push the state-of-the-art, particularly in terms of packaging and in taking advantage of emerging processing methods such as e-beam lithography.

3-D packaging is a novel concept that will be necessary, particularly in mobile technology. As real estate on circuit boards is decreased and the need for shorter interconnects becomes necessary, a 3-D approach can be taken to minimize the chip footprint and interconnect distance and increase reliability. An especially novel concept involves integrating GaN-based high power amplifier devices with established Si-based CMOS technology. Considerable work must be done to solve the processing challenges presented to realize this structure, but the base technology has been well established in other fields. Clearly it is an exciting time to be involved in wide-bandgap semiconductor processing - a time when Si and GaAs are being pushed to their theoretical limits, and nitrides are just beginning to show their potential.
APPENDIX A
EQUIPMENT OPERATION

A.1 Purpose

This chapter is meant to serve as a database of operating procedures for the equipment in Dr. Ren’s labs.

A.2 Spin-Coating

1. Turn on spin coater with power switch.
2. Place the appropriate size chuck on the spinner.
3. Press the foot pedal to activate spinner, check spin speed on digital readout (in kRPM). Adjust using know if necessary. The time readout is on the left and is set to 30s. DO NOT CHANGE THE SPIN TIME.
4. Turn on vacuum pump, place sample on the chuck, perform another test spin to remove any dust particles on the sample.
5. Apply photoresist using disposable pipette. Only a small amount is needed, a drop about ¼ the size of the sample will be more than sufficient (a drop the size of a quarter will coat an entire 4-inch wafer).
6. Press the floor pedal to activate spinning.
7. After the spinner stops, remove the sample with tweezers. Use the ones by the spinner so you do not get photoresist on your personal sample tweezers.
8. Shut down: turn off vacuum pump (sometimes the switch gets dust in it and quits working. If this happens, take the pump to Jim to have it cleaned) and turn off the spinner.

A.3 Mask Aligner (MJB-3)

1. Turn on N2, air compressor at source.
2. Enter clean room and turn on corresponding ball valves.
3. Turn on power to mask aligner and lamp power source.
4. When lamp power source displays “rdy”, press start to fire the lamp. “cold” should appear if the lamp started alright, otherwise it will go back to “rdy.”
5. Allow lamp to warm up (power level will display when it is ready). Prepare photoresist while waiting.
6. Turn on the vacuum pump, load mask on mask holder so that the chrome side will face the wafer, and press “vacuum mask” button to activate the vacuum system on the mask holder.
7. Load the mask holder into the aligner into the slot on the front.
8. Load the wafer by pulling out the slide, placing the wafer in the correct orientation, and sliding back into the system.
9. Put the wafer in contact mode to verify height. The wafer should not move in contact (both handles forward) but should be free in separation mode (back handle forward, front handle back).
10. Perform alignment in separation mode.
11. Place in contact, set correct exposure time, and press “exposure” to perform the exposure
12. Remove the wafer from contact (both handles forward) and develop.
13. Remove the mask by reversing step 6
14. Shut down system: turn off power to aligner, lamp, and vacuum pump, turn off air and N2 ball valves and sources

A.4 Raith E-Beam Lithography

1. Load sample on the appropriate chuck. Use electrostatic chuck for full 4-inch wafers. Make sure at least one clamp is touching the sample for grounding. Make sure the sample is oriented correctly relative to the electron beam, NOT the ccd camera. The SEM image is rotated 90 clockwise relative to the CCD camera.
2. Place the chuck in the system, log in to the software, sample handling window, click load to begin the loading process. This is automated.
3. When loading is completed, the system will ask for a series of values. Typical values are accelerating voltage = 10 kV, aperture size = 30 mm
4. Set up alignment window with proper coordinates (determine from GDS file if necessary) and set the active area in the GDS file.
5. Move to sample so that the edge is approximately under the pole piece of the SEM using CCD camera. This will put the starting point near the sample, but not at risk of accidental exposure.
6. Turn on the SEM (beam on). Adjust focus roughly.
7. Use the SEM to find the first alignment mark. Place the mark roughly at the center of the screen using the crosshairs. Read this point.
8. Use either the SEM or stage translations to find the second and third alignment marks. Read these points to the alignment window. Click “adjust” block to calculate the coordinate transform. I prefer to set up the coordinates roughly first so you do not get lost on the sample.
9. Find a particle on the surface of the resist. It should be small (<5 μm) or have very sharp points (radius <500 nm). Use this to fine tune focus and adjust stigmation and aperture alignment. Remember that in the SEM, anything focused at high magnification will remain focused in low magnification.
10. Use the crosshairs at high magnification to move a clear reference point to the center of the screen. Perform write field alignment at this point.
11. Use the stage translation window to move to the Faraday cup on holder. Turn on the beam and in the beam current window click “measure”. This will read the beam current from the picoammeter.
12. Since the alignment marks have been found, use the lightning bolt icons to move back to each point and fine tune the alignment at a higher magnification. 10-15KX works well for 2-5 μm marks. A good way to do this is to use the annotation to measure out half of the mark width in each direction from center using the crosshairs, then fit the mark to the annotation.
13. Set up the exposure, making sure the dose is set and calculating the other values, check the layer, and click on the “adjust working area” button to ensure that the software will
move the sample to the working area rather than just starting the exposure from where the chuck is located.

14. Begin exposure. The system should handle everything from here, but periodically check on it. The time is about 1.5 times the calculated time.

15. Unload the sample by clicking on the “unload sample” button. The procedure is automated and will take about 10 minutes.

16. Remove the samples from the chuck and place the chuck back in the system.

A.5 Plasma-Therm PECVD

1. Turn on system N2 cylinder
2. Start vacuum pump (master and blower switches)
3. Switch on power supply for the system (next to pump)
4. Turn on chiller: open water lines (supply and return, close crossover valve), press start/stop button
5. Check the system to verify utilities startup – “air,” “water,” “nitrogen,” “+15V,” “-15V,” “+24V” boxes are all green
6. Turn on interlocks at the bottom right of the system in the following order – primary mech pump, lock pump, turn switch to “enable” (machine power switch remains off)
7. Turn off “hold” button on screen and turn on “standby” button
8. Pump the system by going to the “Service” menu, then to “Mainetnance” > “Pump” > “System.” Use the “Windows” pull down menu to access the system overview diagram if necessary, and check the pressure of the chamber. It should be 0 mTorr
9. Load the try into the chamber for heating. Go to the “Service” menu, then “Mainetnance” > “Wafer Handling.” Click on the “Load” button. After the process is complete, click “Exit.”
10. Set the temperature of the chamber. Go to the “Utilities” menu, then “Set Standby Temps.” There is some offset in the software, so a setting of 283 °C will correlate to 255 °C on the temperature controller (lower left cabinet on the front panel of the system). Heating will take 2-3 hours.
11. Turn on the gases required for the reaction. Go to the “Service” menu, then “Mainetnance” > “Evacuate Gas Lines.” Click on the box corresponding to each gas line, wait for evacuation, then turn on the gas. A stable flow should appear. Begin with SiH4, and NEVER evacuate more than one line at a time. The CF4LK line is attached to the N2O cylinder.
12. Set up the system for the reaction. Go to the “Service” menu, then “Manual Mode.” Input the process parameters from the recipes as necessary.
13. Perform a test run - Set the time to 2 min. Click on the “Gas” button to begin gas flow to the chamber, and wait for the flow to stabilize (boxes turn green). Click “Pressure” and wait for the chamber pressure and temperatures to stabilize. Click “RF” to activate the RF power.
14. Click the “Purge” button to purge the chamber with nitrogen after each run. Perform the purge at least 3 times for 1 minute each.
15. Unload the tray and vent the loadlock (“Utilities” menu, go to “Loadlock” > “Vent”)
16. Load a sample and repeat the process. Adjust the process time as per the thickness requirements. It is best to run a test sample and check the thickness using ellipsometry before running a real sample.

17. To shut down the system, begin by turning off the gas lines. Turn off the gas at the cylinder and then use the “Evacuate Gas Lines” procedure to completely evacuate the lines.

18. Close the gate valves on the system (“Utilities” > “Close Gates” > “System”)

19. Set the temperatures back to room temperature

20. Turn off the “Standby” button

21. Close the interlocks and silence the alarm

22. Turn off the pump, power supply, and chiller

23. Turn off the system nitrogen. The last message displayed should be “System Nitrogen Is Low.”

A.6 Evaporator (CHA)

1. Turn on the roughing pump in the chase
2. Close the high vacuum gate valve with the switch and turn off the ion gauge 2.
3. Vent the chamber with the “Vent” switch. Venting is complete when the chamber door can easily be opened. Turn off the vent switch when complete.
4. Load the sample and check the metal levels by opening the shutter and rotating through the crucibles.
5. Pump the chamber by pressing the “Rough” switch.
6. When the pressure is <25 μm Hg, turn off the roughing switch and turn on the high vacuum switch to open the gate valve.
7. Turn off the roughing pump, wait 2-3 hours for the system to achieve high vacuum (<1x10^-6 mTorr)
8. Turn on the chiller, wait ~10 minutes for it to warm up.
9. Turn on the power supply, wait ~10 minutes for it to warm up
10. While waiting, set the deposition parameters as per the log book
11. Turn on the high voltage (key and toggle switch) and the beam sweeper (toggle switch)
12. Use X and Y controls to adjust the beam position to the center of the crucible. The shutter will open after 2 minutes.
13. Monitor the time during deposition. Do not run the system for more than 5 minutes at a time. Always cool down for 5 minutes between depositions.
14. When deposition is complete, wait 10 minutes and then turn off the power supply in the chase. Wait another 10 minutes and turn off the chiller.
15. Vent the chamber, remove the sample, and pump the chamber again.

A.7 Old Evaporator

1. Turn on roughing pump and turbo pump for warm-up
2. Close the high vacuum gate valve
3. Vent the chamber by turning on both nitrogen valves.
4. When gas is escaping the bottom of the bell chamber, venting is complete.
5. Use the hoist to raise the chamber up.
6. Load the sample, lower the hoist
7. Close the nitrogen valves, open the valve to the roughing pump and chamber
8. Wait for the chamber to pump down. Switch to the turbo pump by closing the roughing pump valve opening the valve when the pressure = 100 μm Hg. Turn off roughing pump
9. Wait for the chamber to pump. Switch to the cryo pump by closing the turbo pump valve and chamber valve and opening the gate valve when the pressure = 10 μm Hg. Turn off turbo pump.
10. Wait 4-6 hours for the system to reach high vacuum (pressure < 1x10^-6 mTorr)
11. Turn on chiller, wait 10 minutes for warm up
12. Turn on power supply, wait 10 minutes for warm up. Turn on the deposition controller and set the deposition parameters as per the log book while waiting.
13. Turn on the high voltage (key and push button) and the beam sweep (push button).
14. Verify that the beam position is near the center of the crucible. The beam should not need adjusting.
15. Monitor time during deposition. Do not deposit for more than 5 minutes to avoid damage to the system. Always wait 5 minutes between depositions.
16. When deposition is complete, wait 10 minutes and then turn off the power supply. Wait another 10 minutes and turn off the chiller.
17. Vent the chamber, remove the sample, and pump the chamber again.

A.8 Thermal Evaporator

1. Turn on the control panel, roughing pump and turbo pump
2. Open the ball valves for nitrogen and house chilled water supply and return
3. Vent the chamber using the toggle valve at the system interface
4. Use the hoist toggle switch to raise the chamber top
5. Remove the glass chamber wall and clean with acetone if necessary
6. Load the boat with metal charges and replace the glass wall. The relationship between metal mass loaded and final film thickness is linear, and a calibration curve should be established with all new metals.
7. Lower the chamber top and begin roughing the chamber by turning the 3-way valve to the rough position
8. When the chamber pressure reaches 100 μm Hg, change the 3-way valve to the foreline position, wait a minute to pump out the line, and then open the turbo pump valve
9. Turn on the high vacuum gauge. Wait for the chamber to pump down (<1x10^-5 mTorr)
10. To deposit, turn on the current supply. Manually ramp up the current. Dwell for 1 minute at a low setting relative to the deposition current for initial heating.
11. Slowly ramp the current to an intermediate setting and watch the metal charge for melting. Dwell until the charge is completely melted.
12. Ramp the current to the deposition level and open the shutter. Evaporate the entire charge.
13. Slowly ramp down the current supply, turn it off and wait 5 minutes for cooling.
14. Turn off the turbo pump valve, turn the 3-way valve to off, and vent the chamber.
15. Clean the chamber wall and pump the chamber.
APPENDIX B
ELECTRICAL MEASUREMENTS

B.1 Purpose

This section is meant to provide information on the standard electrical measurements that are performed to quantify HEMT performance. Background and system setup diagrams will be given when applicable. A thorough knowledge of electrical testing is a useful tool. Just as much diagnostic information, if not more, can be gathered from a round of electrical testing as from a full battery of analytical equipment.

B.2 Ohmic Contacts

B.2.1 Overview

Transmission Line (TLM) testing is used to quantify the ohmic contacts. A typical transmission line consists of a series of ohmic contacts with varying spacing on one mesa. By measuring the current-voltage curve between each contact, one can calculate the resistance from Ohm’s Law (V=IR) as the simple slope of the line. The resistance is a linear function of the spacing between contacts, so from here one can fit a curve if these values are plotted. The resulting slope will be the sheet resistance ($R_s$), which is reported in ohms/sq. This is the resistance purely of the semiconductor material. In an ideal situation, the intercept of this line will be zero, but since the contacts themselves have some resistance, the slope will represent the transfer resistance ($R_T$), which is reported in ohm/mm. These factors are combined into a specific contact resistance ($R_c$), which is defined as $R_s/R_T$, and is reported in ohm-cm$^2$. A good ohmic contact will have $R_c \sim 1 \times 10^{-6}$ ohm-cm or smaller.

B.2.2 Procedure

An optical image of a TLM pattern is shown in Figure B-1 to demonstrate the terminals. Use the parameter analyzer and probe station for this test, as shown in Figure B-2. Set up the
parameter analyzer for a diode (Vf-If) measurement. A typical test range is from –1 V to 1 V. Probe the TLM pads, starting with the largest spacing. Determine the slope of each line (the intercept should be zero). This can be done by either curve fitting in Excel after testing, as shown in Figure B-3, or directly measuring the tangent on the parameter analyzer. The resistance is equal to 1/slope from Ohm’s Law (\(V=IR\), therefore \(R=V/I\)). Plot the resistance as a function of the gap between pads, as shown in Figure B-4. Perform a linear fit to determine the slope and the intercept of this line. The sheet resistance \(R_s\) is equal to 100*slope. The transfer resistance \(R_T\) is equal to intercept*0.1/2. The 0.1 comes from the pad length, in mm, and the 2 comes from the number of pads.

**B.3 Direct Current**

**B.3.1 Overview**

DC testing is performed to check for basic function of HEMTs. This primarily means checking for current saturation and gate modulation. To this end, two curves are typically taken – source-drain voltage vs source-drain current at varying gate voltages and gate voltage vs source-drain current at a constant drain voltage. The former measurement is used to check for saturation, and the latter used to check the gate characteristics.

Ideally, the current will linearly increase at low voltages and then level off at saturation. In sapphire or Si HEMTs, the current will actually decrease linearly with increasing drain voltage past the saturation voltage. This is due to the self-heating of the device, and therefore is not seen in SiC HEMTs. By extrapolating the linear region forward and the saturation level back, the knee voltage can be found as the intersection of these lines. Knee voltage is a function of gate to drain distance, and thus increases linearly with this gap. The current level is typically normalized and reported as mA/mm or A/mm, where mm refers to the total gate width. A state-of-the-art GaN HEMT approaches the theoretical limit of 1.2 A/mm. This test is also used to check for gate
modulation. In a depletion mode device, the gate voltage is modulated from 0 in steps of -1 V until pinch-off is reached. The current saturation level should decrease with increasing reverse gate bias. Typically pinch-off occurs between -2 and -7 V, and if nothing is reached by -10 V, there is most likely a problem with the gate of the device.

The second curve taken is the gate voltage vs drain current curve. Typically the gate voltage is taken from beyond pinch-off (-10 V, for example) to 0.5 V. One should see the drain current leveling off beyond \( V_g = 0 \), so this is why it is taken to slightly beyond 0. The drain current should linearly decrease with increasing reverse gate bias as pinch-off is approached, and be nearly flat at a very low current level (nA) beyond pinch-off. A line can be extrapolated back to the x-axis to determine the threshold voltage. The transconductance (\( g_m \), reported normalized as mS/mm or S/mm) can also be determined from this curve. It is defined as \( \frac{dI}{dV} \), so it amounts effectively to the first derivative of this curve. It can be calculated manually by calculating \( dI \) and \( dV \) between two consecutive points for the entire curve. A good maximum \( g_m \) is above 200 mS/mm, which implies a very sharp transition from on to off states.

**B.3.2 Procedure**

An optical image of a HEMT is shown in Figure B-5 to demonstrate the terminals. Use the parameter analyzer and probe station for this test, as shown in Figure B-6. Set up the parameter analyzer first for FET \( V_d-I_d \) measurement. The drain bias range depends on the source-drain spacing, but 0-10 V is typically a good starting point. For a depletion mode device, the gate should go from 0 to pinch-off in –1 V steps. If the pinch-off voltage is not known, -5 or –6 V is a good starting point. A sample curve is shown in Figure B-7.

After performing this measurement, change the measurement mode to FET \( V_g-I_d \) measurement. The drain bias will be constant in this mode, and should be set to just beyond
saturation (5 or 6 V in the sample curve) and the gate voltage should be set beyond pinch-off (-10 V is typically good). A sample curve is shown in Figure B-8.

### B.4 Pulse (Gate Lag)

#### B.4.1 Overview

A pulsed gate test is used to look at traps in the semiconductor material. In this measurement, the gate voltage is pulsed from beyond pinch-off to on at a given rate (typically 1 kHz-1 MHz range) and at a given drain bias. The traps in the material, particularly surface states and buffer traps, will cause the system to respond differently to a pulsed gate as opposed to DC operation. This measurement is used to generate the same curves as DC measurements so that a direct comparison can be made. A high density of surface states is manifested as a low drain current under pulsed conditions as compared to DC (under 80%). A high density of buffer traps is manifested as a shift in threshold voltage under pulsed conditions (as much as 2 V or more).

#### B.4.2 Procedure

A schematic of the test setup is shown in Figure B-9. A DC power supply is used to apply source-drain bias. A resistor of known value is then used to back out the current from Ohm’s Law. There will be a voltage drop across the resistor, measured by the voltage at the power supply compared to the voltage measures on screen at the oscilloscope. Therefore, from \( V = IR \), \( I = \frac{\Delta V}{R} \). It is important to choose a resistor that will provide the appropriate sensitivity so that the voltage drop can be measured, but is not so large that significant digits are lost. Typical values are 10 \( \Omega \) and 48 \( \Omega \). The gate voltage is supplied from the pulse generator, pulsing from pinch-off (typically –10 V) to the desired gate voltage with a 10% duty cycle. This type of test setup means that every point must be calculated as there is no automated measurement on this system.
When measuring the Vd-Id curve, typically only the Vg = 0 curve is used. The pulse will therefore be from -10 V to 0 V. To take the point at Vd = 1 V, the oscilloscope center line is set at 1 V (note that this is before the resistor so this will be the true drain voltage), the pulse is turned on, and the DC power supply is ramped up so that the bottom of the pulse step is at the center line. The reading on the DC power supply is recorded for current calculation. This process is repeated for each point that one wishes to measure. Typically the drain voltage step is 1 V. A typical curve relative to the DC curve is shown in Figure B-10.

To measure the Vg-Id curve, the oscilloscope center is set at the same voltage that the DC Vg-Id curve was taken at. The pulse magnitude is changed to the various gate voltages that one intends to measure. For example, starting at a pulse from –10 V to 0 V, the next step may be say –10 V to –0.5 V, and so on. Typical step size is –0.5 or –0.25 V. At each step, the DC power supply voltage is adjusted so that the bottom of the pulse falls at the center line. The same current calculation applies. A typical curve is shown in Figure B-11.

**B.5 Leakage/Isolation**

**B.5.1 Overview**

The source-gate and gate-drain Schottky diodes are used to check for gate leakage. The characteristics should match an ideal diode. The isolation can be tested between ohmic contacts on two adjacent mesas. If mesa etching was successful in confining the 2DEG, the isolation current will be very low (nA). If the current between two adjacent mesas is high (μA-mA), further etching is required. Leakage testing is essentially diode characterization. The source-gate or drain-gate diode is tested, and a low current level and good turn-on are ideal.

**B.5.2 Procedure**

Isolation testing is set up like TLM testing, and the two are typically performed at the same time. The difference is where a TLM pattern is measured between ohmic pads on the same mesa,
isolation is measured between adjacent mesas. If the mesa has not been etched deep enough, current will flow between the two mesas (mA level). If the mesa has been sufficiently etched to confine the electrons, there will be no current flow (nA level). A typical voltage range for this measurement is –40 V to 40 V. A good isolation curve is shown in Figure B-12. When designing a mask, it is desirable to put a set of pads on separate mesas close to each other (10-20 μm) for isolation measurements.

A schematic for a diode measurement is shown in Figure B-13. This measurement uses the parameter analyzer in diode (Vf-If) mode. Forward and reverse bias measurements should be made separately to avoid damaging the device. Forward bias should never exceed 5 V, and reverse should never exceed –10 V. It is important to set the compliance level very low (<10 mA forward, <1 mA reverse) to avoid damage. The ohmic pad (SMU3 – source or drain) is ground. A typical curve for forward bias is shown in Figure B-14.

**B.6 Breakdown/High Power**

**B.6.1 Overview**

High power testing is typically used to check the breakdown voltage of HEMTs. Extreme care must be taken to protect the tester and the device as much as possible. Testing is usually performed in Fluoroinert for high breakdown devices. The breakdown of air occurs around 400 V, so this solution, which is a Teflon-based liquid, will allow for testing beyond this level. Typically the device is operated at or near pinch-off to prevent damage and to obtain the true breakdown voltage of the material. The current level will be either flat or slightly increasing, then demonstrate a sharp increase at the breakdown voltage. In an ideal careful test, one can approach this voltage slowly and just reach the breakdown point and stop before the device arcs and is destroyed.
B.6.2 Procedure

Breakdown measurements below 400 V can be performed with the curve tracer, as shown in top of Figure B-15. On this system, the compliance setting is a power level, so it is a combination of current and voltage. Therefore the compliance can be reached at high current and low voltage or high voltage and low current. While the compliance on this system will protect the system, it can still create hazardous voltages or currents to the user. Set the sweep for a DC Vd-Id measurement. It is best then to begin at the lowest settings and gradually work up. The sweep is set to go from high to low power, and is represented at a percentage of maximum power. Therefore the setting should be gradually increased, with single measurements, and then when the desired point is reached, a sweep back can be used to obtain the full I-V curve. The curve that is generated is shown in Figure B-16.

If the breakdown voltage is too high to measure with the curve tracer, the Glassman High Voltage power supplies can be used. A DC power supply must be connected to the system to control the voltage. An applied voltage of 0-10 V will correspond to 0-max power (1 kV, 6 kV, 20 kV) on the high voltage supply. The high voltage is connected to the drain terminal through a large (1 MΩ) resistor to limit the current for safety. The source terminal is connected to a digital multimeter to measure the source-drain current. The gate voltage is controlled through a second DC power supply to maintain the gate voltage near pinch-off. The breakdown is determined by monitoring the current level and looking for a sudden sharp rise. A schematic of the test system is shown in the bottom of Figure B-15.

B.7 Small Signal RF (S-parameters)

B.7.1 Overview

This test is used to look at the frequency response of a HEMT. It inputs a small RF signal over a large frequency range (typically 10 MHz to 40 GHz or more) and measures what are
referred to as the s-parameters, which have both a real and imaginary component on a Smith chart. From these, several different gain modes can be calculated. In particular, the unitary gain cutoff frequency (H21) and the maximum gain (U) are calculated and plotted against frequency. At the point where each of these respective curves reaches zero gain, Ft and Fmax are recorded. These values will be a function of gate and drain DC voltage as well. Typically they are maximized when Vd is at saturation and Vg is at the point where Gm is maximized (typically Id = 25% Isat)

The device s-parameters can be simulated using an equivalent circuit model to look at the parasitic resistances and capacitances in the device structure. By inputting the measured data and then using the simulation to attempt to match this data, one can extract the values for the parasitics in the system.

**B.7.2 Procedure**

First, the RF cables and Ground-Signal-Ground (GSG) probes must be connected. Care must be taken as RF components are very sensitive to dust. The DC bias must be set-up to be supplied either through a Bias Tee or through the network analyzer. A schematic of the test setup is shown in Figure B-17. After starting up, the network analyzer must be calibrated and the frequency range must be set. A typical range is 50 MHz-40.05 GHz. Calibration is achieved using the SOLT method (short, open, load, through). The s-parameters are taken with the probes in each configuration (open = probes lifted, or in individual pads, short = ground and signal shorted, load = 50 Ω load between signal and ground, and through= probe 1 and probe 2 are connected via transmission lines). A calibration standard with each pattern is available. It is best to change the viewing options to a smith chart to verify calibration. An open probe will be at the
far left of the smith chart (infinite resistance), short will be on the far right (0 resistance), and
load will be in the center (50 Ω resistance).

After calibration, the device is placed on the probe station, oriented with the gate towards
port 1 and the drain towards port 2. After lowering the probes, a DC I-V curve is measured to
ensure that the device is active. The RF measurement is performed using MMICAD software.
After initializing the software to connect to the network analyzer, perform a 2-port measurement.
The software program (HEMT.ckt) will calculate U and H21 and plot a smith chart and the U,
H21, and Gain as a function of frequency. It will also model the equivalent circuit with
parameter estimates. A sample s-parameter plot is shown in Figure B-18, with data in red and
blue, and model in green and brown. A sample frequency plot is shown in Figure B-19, with the
locations of F_T and F_max. If either parameter is beyond the range of the instrument, as in this case,
a line is extrapolated from the last point to the axis with a slope of –20 dB/decade.

**B.8 Large Signal RF (Load-Pull)**

**B.8.1 Overview**

This test is used to look at the power output of a HEMT. In a load-pull test, RF power is
input at a fixed frequency and the output power is measured. The curve produced is input power
vs output power, going from low to high power. From this curve, one can calculate the actual
gain of the device (Pout/Pin) and the power added efficiency (PAE). Note that this measurement
uses the dBm unit scale, which is a logarithmic absolute power unit, standing for a decibel
referenced to 1 mW power (1 dBm = 1 mW, 10 dBm = 10 mW, -10 dBm = 0.01 mW). A typical
curve is shown in Figure. The gain is usually linear over a large range, then begins to decrease as
the power output saturates. This point is referred to as the compression point. Each dB below the
constant gain level is referred to as a dB of compression. Typically devices are operated at the 1-
3 dB compression range.
Typically this measurement requires an RF source that has the capability to set a single frequency with variable power, power meters at least for input and output (some systems also use reflected power to measure the true power input to the system), tuners for impedance matching, and a DC bias system. A considerable amount of time must be put into this measurement, as each component must be measured and calibrated out so that only the characteristics of the device are calculated.

B.8.2 Procedure

A schematic of the load-pull system is shown in Figure B-20. All components must be calibrated first in order to make the measurement. This process can take several days. First, the network analyzer must be started and calibrated as described in the previous section. The tuners are then connected to the network analyzer for calibration. S-parameters are taken at specified impedance points on the tuner. This procedure typically takes 8-10 hours per tuner as the tuner must move to each position. The Maury load-pull software manages all of the data acquired. The power meters must be set to the correct frequency, and it is best that they are zeroed as well. S-parameters are taken for the directional coupler, power meters, bias tees, and probe tips. All of this data is assembled by the Maury software for calibration.

When a device is placed on the probe station, a DC curve is taken first. The tuners must then be moved to perform impedance matching. When the input and output impedance is matched, the DC bias is then applied, and then RF power is applied. A sweep is performed to measure input and output power as a function of the input power from the RF generator. Input and output power and gain are then plotted as a function of input power for the device. A typical curve is shown in Figure B-21. While most of this is performed by the software, it is important to note that the dB scale is logarithmic, so while gain is defined as the difference between output and input power, this cannot be calculated in dB. The power must be converted to mW,
subtracted, and then converted back to dB. The correlation is $P_{\text{dBm}} = 10 \log(P_{\text{mW}})$, or reversed, $P_{\text{mW}} = 10^{\frac{P_{\text{dBm}}}{10}}$. 
Figure B-1. Optical image of TLM pattern.

Figure B-2. Test setup for TLM measurement
Figure B-3. Typical I-V curves for TLM measurement

Figure B-4. Calculation of Rs, Rt, and Rc from TLM measurement
Figure B-5. Optical image of GaN HEMT

Figure B-6. Test setup for DC measurement

To source ——— SMU1
To drain ——— SMU2
To gate ——— SMU3

Agilent 4156
Parameter Analyzer
Figure B-7. Typical DC $V_{ds}$-$I_{ds}$ curve

Figure B-8. Typical DC $V_{gs}$-$I_{ds}$ curve
Figure B-9. Test setup for gate lag measurement

Figure B-10. Typical pulsed Vds-Ids curve compared to DC
Figure B-11. Typical pulsed Vg-Ids curve compared to DC

Figure B-12. Typical isolation data
Figure B-13. Schematic of test setup for gate leakage measurement

Figure B-14. Typical leakage data
Figure B-15. Test setup for breakdown measurement <400 V (top) and >400 V (bottom)
Figure B-16. Typical breakdown data

Figure B-17. Test setup for small signal RF measurement
Figure B-18. Typical s-parameter data

Figure B-19. Typical H21 and U calculation for Ft and Fmax
Figure B-20. Test setup for load-pull measurement

Figure B-21. Typical load-pull data
APPENDIX C
PROCESSING RECIPES

C.1 Purpose

This appendix is meant to serve as a database of processing recipes. There may be more than one recipe that works for any given process, so this is by no means a definitive set. It does, however, represent a list of recipes that have consistently worked for me over the years.

C.2 Photolithography

C.2.1 Mesa Etching (S-1045)

1. Spin 1045, 3000 RPM, 30s
2. Soft bake for 5 minutes at 110 °C (hot plate)
3. Expose for 30 sec, develop 20s in MF-322
4. Hard bake 15 minutes, 110 °C (hot plate)

C.2.2 Lift-Off (S-1818)

1. Spin 1818, 4000 rpm, 30s
2. Soft bake 110 °C, 5 min
3. Toluene soak, 30s, N2 dry
4. Expose 25s, develop 30s in MF-321

C.2.3 Lift-Off (S-1808)

1. Spin 1808, 4000 RPM, 30s
2. Soft bake for 1 minute at 80 °C (hot plate)
3. Soak in toluene for 1.5 minutes
4. Soft bake for 10 minutes at 90 °C (oven)
5. Expose for 15 sec, develop for 1 minute in MF-321
6. Descum in O2 plasma for 1 min
7. Remove oxide using 5% HCl or BOE for 1 min

C.2.4 Lift-Off (LOR/1808)

1. Spin LOR, 5000 RPM, 30s
2. Soft bake 150 °C, 2 min
3. Spin 1808, 5000 RPM, 30s
4. Soft bake 110 °C, 5 min
5. Expose 30s, develop 15s in MF-321
6. Descum in O2 plasma for 1 min
7. Remove oxide using 5% HCl or BOE for 1 min
C.2.5 Image Reversal (5214)

1. spin 5214, 4000 RPM, 30s
2. soft bake, 100 °C, 1.5 min (oven)
3. expose 10s with mask
4. bake, 110 °C, 2 min (hot plate)
5. flood expose, 30s
6. develop 30s in AZ400K:H2O (1:4)
7. hard bake, 110 °C, 30 min (oven)

C.2.6 Air Bridge

1. spin PMGI, 3000 RPM, 30s
2. soft bake, 180 °C, 20 min
3. spin 1045, 3000 RPM, 30s
4. soft bake, 110 °C, 5 min
5. expose 25s, develop 45s in MF-322
6. hard bake, 110 °C, 15 min
7. Etch PMGI in O₂ plasma
8. Remove photoresist in acetone
9. Bake at 180 °C for 1 hour to round the edges of the PMGI
10. Deposit seed Au layer in evaporator (1000 A)
11. Pattern air bridge level using 1045 resist (see previous section for processing)
12. Electroplate Au (~5 μm) in opened areas
13. Remove photoresist with acetone
14. Remove seed layer by plasma etching

C.3 E-Beam Lithography

C.3.1 Etching (PMMA)

1. Spin PMMA to desired thickness (2% = ~1000, 4% = ~2000), 4000 RPM, 30s
2. Remove photoresist form one corner for conductivity in the SEM using acetone
3. Soft bake, 195 °C, 10 min
4. Expose at 10 kV, 100 μC/cm²
5. Develop 30s in MIBK:IPA (1:3), Rinse with IPA

C.3.2 Lift-off (PMMA/PMMA-MAA)

1. Spin PMMA-MAA copolymer to desired thickness (7% = ~2000), 4000 RPM, 30s
2. Remove photoresist from one corner for conductivity in the SEM using acetone
3. Soft bake, 195 °C, 10 min
4. Spin PMMA to desired thickness (2% = ~1000, 4% = ~2000), 4000 RPM, 30s
5. Remove photoresist from one corner for conductivity in the SEM using acetone
6. Soft bake, 195 °C, 10 min
7. Expose at 10 kV, 100 μC/cm²
8. Develop 30s in MIBK:IPA (1:3), Rinse with IPA

**C.3.3 T-gate (PMMA/PMMA-MAA/PMMA)**

1. Spin 4% PMMA, 4000 RPM, 30s
2. Remove photoresist from one corner for conductivity in the SEM using acetone
3. Soft bake, 195 °C, 10 min
4. Spin 7% PMMA-MAA copolymer, 4000 RPM, 30s
5. Remove photoresist from one corner for conductivity in the SEM using acetone
6. Soft bake, 195 °C, 10 min
7. Spin 2% PMMA, 4000 RPM, 30s
8. Remove photoresist from one corner for conductivity in the SEM using acetone
9. Soft bake, 195 °C, 10 min
10. Expose at 30 kV, 70 μC/cm2
11. Expose at 30 kV, 130 μC/cm2
12. Soak in chlorobenzene, 6s
13. Develop 60s in Methanol:IPA (1:1)
14. Develop 30s in MIBK:IPA (1:3), Rinse with IPA

**C.4 Plasma Etching**

**C.4.1 Inductively Coupled Plasma Etch With Cl₂ (AlGaN/GaN and Au)**

Temp = 25 °C  
Pressure = 2 mTorr  
ICP Power (RF2) = 150 W  
RF Power (RF1) = 40 W  
Gas flows: Cl₂ = 10 sccm  
Ar = 5 sccm  
Etch Rate = ~800 A/min for GaN (strongly dependent on material quality)  
~1500 A/min for Au

**C.4.2 Reactive Ion Etch With CF₄ (SiO₂, Si₃N₄)**

Temp = 25 °C  
Pressure = 175 mTorr  
RF Power = 50 W  
Gas flows: CF₄ = 50 sccm

**C.4.3 Reactive Ion Etch With O₂ (polymers)**

Temp = 25 °C  
Pressure = 315 mTorr  
RF Power = 50 W  
Gas flows: O₂ = 30 sccm
C.5 Plasma Enhanced Chemical Vapor Deposition

C.5.1 Silicon Nitride (SiNx)

Temp = 255 °C  
Pressure = 900 mTorr  
RF Power = 30 W  
DC Bias = 0  
Ref Power = 0  
Gas flows: SiH4 = 100  
N2 = 400  
NH3 = 27  
Dep Rate = ~115 A/min  
Refractive index = ~1.7-1.9

C.5.2 Silicon Dioxide (SiO2)

Temp = 255 °C  
Pressure = 900 mTorr  
RF Power = 30 W  
DC Bias = 0  
Ref Power = 0  
Gas flows: SiH4 = 200  
N2O = 200  
Dep Rate = ~300 A/min  
Refractive index = ~1.38-1.46

C.6 Wet Etching

C.6.1 Buffered Oxide Etch (SiNx, SiO2)

SiNx etch rate = ~1000 A/min  
SiO2 etch rate = ~6000 A/min  
Aqua Regia (Ni)  
Formulation = HNO3:HCl:H3PO4 (3:1:1)  
Ni etch rate = ~1 μm/min

C.7 Thermal Evaporation

C.7.1 Indium

Current = 200 A  
Deposition Rate = 125 A/s  
1 In charge = ~1 μm film
C.8 Flip-Chip Bonding

C.8.1 Indium-Gold

- Pressure = 200g for contact, 400g during heating
- Temperature = 174 °C
- Time = 10 min

C.8.2 Gold-Gold

- Pressure = 1.3 kg
- Temperature = 375 °C
- Time = 10 min

C.8.3 Polymer (SU-8-SU-8)

- Pressure = 1 kg
- Temperature = 135 °C
- Time = 10 min
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BIOGRAPHICAL SKETCH

Travis James Anderson, a native of Miami, Florida, began his higher education at the Georgia Institute of Technology in Atlanta, GA, where he had the opportunity to work as a research assistant for a prominent faculty member. After garnering much experience, he graduated from Tech in May 2004 with a bachelor’s degree in chemical engineering. That fall, Travis enrolled in the Ph.D. program in the Chemical Engineering Department at the University of Florida to further explore his research interests. In spring 2005, he joined Dr. Fan Ren’s research group and began the substantive research used to develop this dissertation. Since joining the group Travis’ research has focused largely on the maturation of compound semiconductor device technology, studying novel sensors and transistors, systems integration, and reliability. Having attained a high level of proficiency in this research area, Travis graduated in May 2008, with a Doctor of Philosophy in chemical engineering.